

PROJECT NAME :
For Bullseye : GDM54/GDM5D

PCB NO : LA-L245P

Dell / Compal Confidential

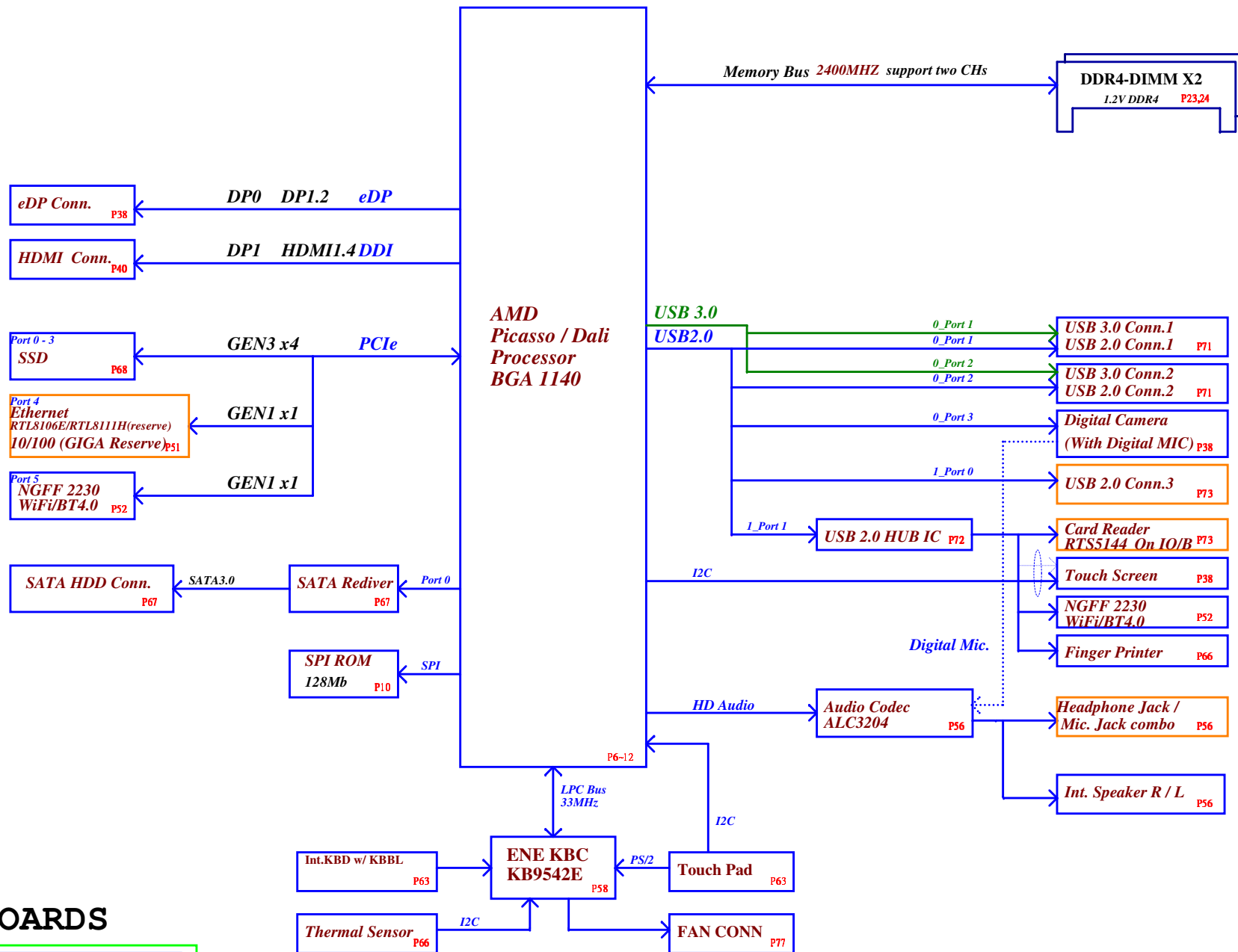
Schematic Document

AMD FP5
Picasso / Dali

2021-03-31 Rev: 1.0 (A00)

Component
LBIST@/LBIST@RF@ : LBIST for LCD monitor

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Issued Date	2016/01/07	Deciphered Date	2017/01/07	Title	P001-Cover Page	
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SUB-BOARDS

I/O & PWR & LAN & Audio & Card reader Board

I/O & PWR & Audio & Card reader Board

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BOM Config

Un-pop :@

-----CPU-----

Picasso APU R1 PN : R3_PICA_R1@/R5_PICA_R1@/R5_PIC3450_R1@/R7_PICA_R1@
Picasso APU R3 PN : R3_PICA_R3@/R5_PICA_R3@/R5_PIC3450_R3@/R7_PICA_R3@
Dali APU R1 PN : 2C2T_DALI_R1@/2C4T_DALI_R1@/R3_DALI_R1@
Dali APU R3 PN : 2C2T_DALI_R3@/2C4T_DALI_R3@/R3_DALI_R3@
BIOS CPU Strap Pin : PICA@/DALI@
Audio SKU Strap Pin: Realtek@/Cirrus@

-----PCB-----

MB PN :PCB@

-----System-----

HDMI Logo :45@

SATA Redriver :TI@/PARADE@/NRDSA@

Touch PAD :TP_WAKE@/PTP@/NPTP@

KB BackLight :KBBL@

Touch Screen :USBTCH@/I2C0TCH@/I2C3TCH@

AMD Debug :HDT@

Power Switch :EVTSW@

EMI,ESD,RF :EMI@/ESD@/RF@

EMI,ESD,RF unpop :@EMI@/ESD@/RF@

Picasso Phase:P_EVT@/P_DVT1@/P_DVT2@/P_PVT@

Dali Phase:D_EVT@/D_DVT1@/D_DVT2@/D_PVT@

LBIST for LCD monitor:LBIST@/LBIST@RF@

TPM:TPM@/CTPM@/NTPM@

-----No Use Config-----

@

Moderr standby :MODS@

EC reserve :9022@

Connector :CONN@

Board ID Table for AD channel

Vcc	3.3V +/- 1%				
Ra	100K +/- 1%				
Board ID	Rb	V _{AD, pin} min	V _{AD, pin} typ	V _{AD, pin} max	EC AD3
0	0	0.000V	0.000V	0.300V	0x00 - 0x13
1	12K +/- 1%	0.347V	0.347V	0.360V	0x14 - 0x1E
2	15K +/- 1%	0.423V	0.430V	0.438V	0x1F - 0x25
3	20K +/- 1%	0.541V	0.550V	0.559V	0x26 - 0x30
4	27K +/- 1%	0.691V	0.702V	0.713V	0x31 - 0x3A
5	33K +/- 1%	0.807V	0.819V	0.831V	0x3B - 0x45
6	43K +/- 1%	0.978V	0.992V	1.006V	0x46 - 0x54
7	56K +/- 1%	1.169V	1.185V	1.200V	0x55 - 0x64
8	75K +/- 1%	1.396V	1.414V	1.430V	0x65 - 0x76
9	100K +/- 1%	1.634V	1.650V	1.667V	0x77 - 0x87
10	130K +/- 1%	1.849V	1.865V	1.881V	0x88 - 0x96
11	160K +/- 1%	2.015V	2.031V	2.046V	0x97 - 0xA4
12	200K +/- 1%	2.185V	2.200V	2.215V	0xA5 - 0xAF
13	240K +/- 1%	2.316V	2.329V	2.343V	0xB0 - 0xB7
14	270K +/- 1%	2.395V	2.408V	2.421V	0xB8 - 0xBF
15	330K +/- 1%	2.521V	2.533V	2.544V	0xC0 - 0xC9
16	430K +/- 1%	2.697V	2.697V	2.697V	0xCA - 0xD4
17	560K +/- 1%	2.791V	2.800V	2.808V	0xD5 - 0xDD
18	750K +/- 1%	2.905V	2.912V	2.919V	0xDE - 0xF0
19	NC	3.000V	3.000V	3.300V	0xF1 - 0xFF

BOARD ID Table

Board ID	EC AD3
0	Picasso EVT UMA
1	Picasso DVT1 UMA
2	Picasso DVT2 UMA
3	Picasso Pilot UMA
4	Dali EVT UMA
5	Dali DVT1 UMA
6	Dali DVT2 UMA
7	Dali PVT UMA
8	
9	
10	
11	
12	
13	
14	
15	
16	
17	
18	
19	

Voltage Rails

Power Plane	Description	S0	S3	S4/S5
DC_IN	Adapter power supply	N/A	N/A	N/A
+13.2V_BATT+	Battery power supply	N/A	N/A	N/A
+19VB	AC or DC for power circuit	N/A	N/A	N/A
+APU_VDDCORE	Core voltage for APU	ON	OFF	OFF
+APU_VDDSOC	VDDSOC voltage for APU	ON	OFF	OFF
+3VALW_APU	3V always for APU	ON	ON	ON*
+0.9VALW_APU	0.9V always for APU	ON	ON	ON*
+1.8V_ALW_APU	1.8V always for APU	ON	ON	ON*
+0.9VS	0.9V sustain for APU	ON	OFF	OFF
+VGA_CORE	VGA core power rail for GPU	ON	OFF	OFF
+1.35V_MEM GFX	+1.35VS power rail for GPU and VRAM	ON	OFF	OFF
+3VGS	+3VS power rail for GPU	ON	OFF	OFF
+1.8VGS	+1.8VS power rail for GPU	ON	OFF	OFF
+0.9VSDBGPU	0.9SV power rail for GPU	ON	OFF	OFF
+13.2V_VDD_SOC	3.3V power rail for RD chip	ON	OFF	ON*
+3VALW	System +3VALW always on power rail	ON	ON	ON*
+3VLP	+19VB to +3VLP power rail for suspend power	ON	ON	ON
+3VS	System +3VS power rail	ON	OFF	OFF
+0.6V_DDR_VTT	DDR +0.6VS power rail for DDR terminator	ON	OFF	OFF
+1.2V_DDR	DDR4/L-RS +1.2V power rail	ON	ON	OFF
+2.5V_MEM	DDR4/L-RS +2.5V power rail	ON	ON	OFF
+1.8VS	System +1.8VS power rail	ON	OFF	OFF
+5VALW	System +5VALW power rail	ON	ON	ON*
+5VS	System +5VS power rail	ON	OFF	OFF
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF

PCI EXPRESS(GFX)

Lane 1	PEG (AMD)M2-50 (Reserve)
Lane 2	PEG (AMD)M2-50 (Reserve)
Lane 3	PEG (AMD)M2-50 (Reserve)
Lane 4	PEG (AMD)M2-50 (Reserve)
Lane 5	RV2 NA
Lane 6	RV2 NA
Lane 7	RV2 NA
Lane 8	RV2 NA

CLOCK SIGNAL

CLKOUT_PCIE0	dGPU (Reserve)
CLKOUT_PCIE1	10/100 LAN (GIGA Reserve)
CLKOUT_PCIE2	NGFF Card (WLAN)
CLKOUT_PCIE3	NVME SSD

RV2 NA	USB3.0	
	0_Port0	N/A
	0_Port1	USB3 connector 1
	0_Port2	USB3 connector 2
	0_Port3	
	1_Port0	
	1_Port1	
	USB2.0	
	0_Port0	N/A
	0_Port1	USB connector 1
ULT	0_Port2	USB connector 2
	0_Port3	Camera
	1_Port0	USB connector 1 (DB)
	1_Port1	USB HUB
	PCI EXPRESS(GPP)	
	Lane 1	NVME SSD
	Lane 2	NVME SSD
	Lane 3	NVME SSD
	Lane 4	NVME SSD
	Lane 5	10/100 LAN(GIGA RESERVE)
RV2 NA	Lane 6	NGFF Card (WLAN)
	Lane 7	use sata interface
	Lane 8	use sata interface
	SATA	
	SATA0	HDD
	SATA1	N/A

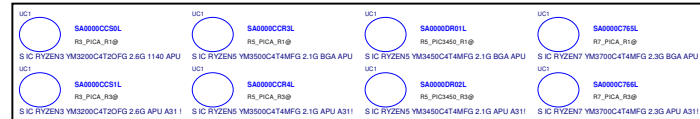
RV2 sata only

RV2 sata only

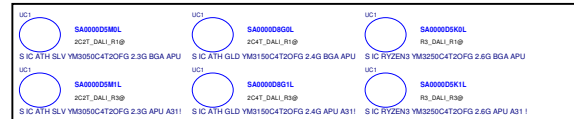
SBUS Control Table

	SOURCE	BATT	Charger	DI90	(G46)	Thermal Sensor	FFS	GPU	APU	EC	TP	TS
EC_SMB_CK1 EC_SMB_DAL1	KB9542E	V	V									
EC_SMB_CK2 EC_SMB_DAL2	KB9542E			V		V	V					
EC_F82_TPCLK EC_F82_TPCLK1	KB9542E										V	
APU_SCLK0 APU_SDAT0	APU			V								
I2C_3_SCL I2C_3_SDA	APU				V						V	V
APU_SIC APU_SIO	APU			V		V		V				

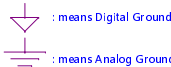
Picasso APU



Dali APU

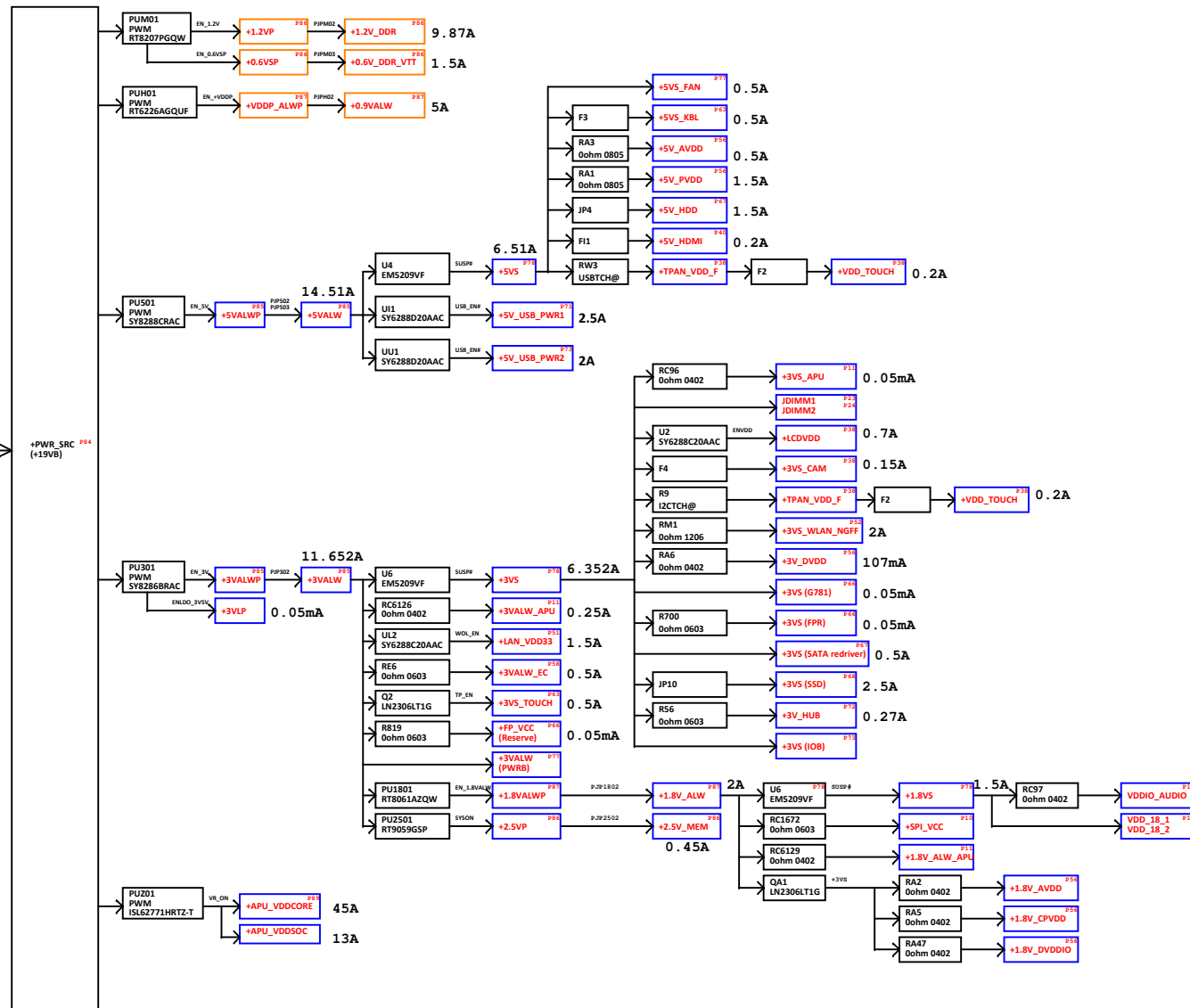
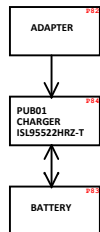


Symbol Note :



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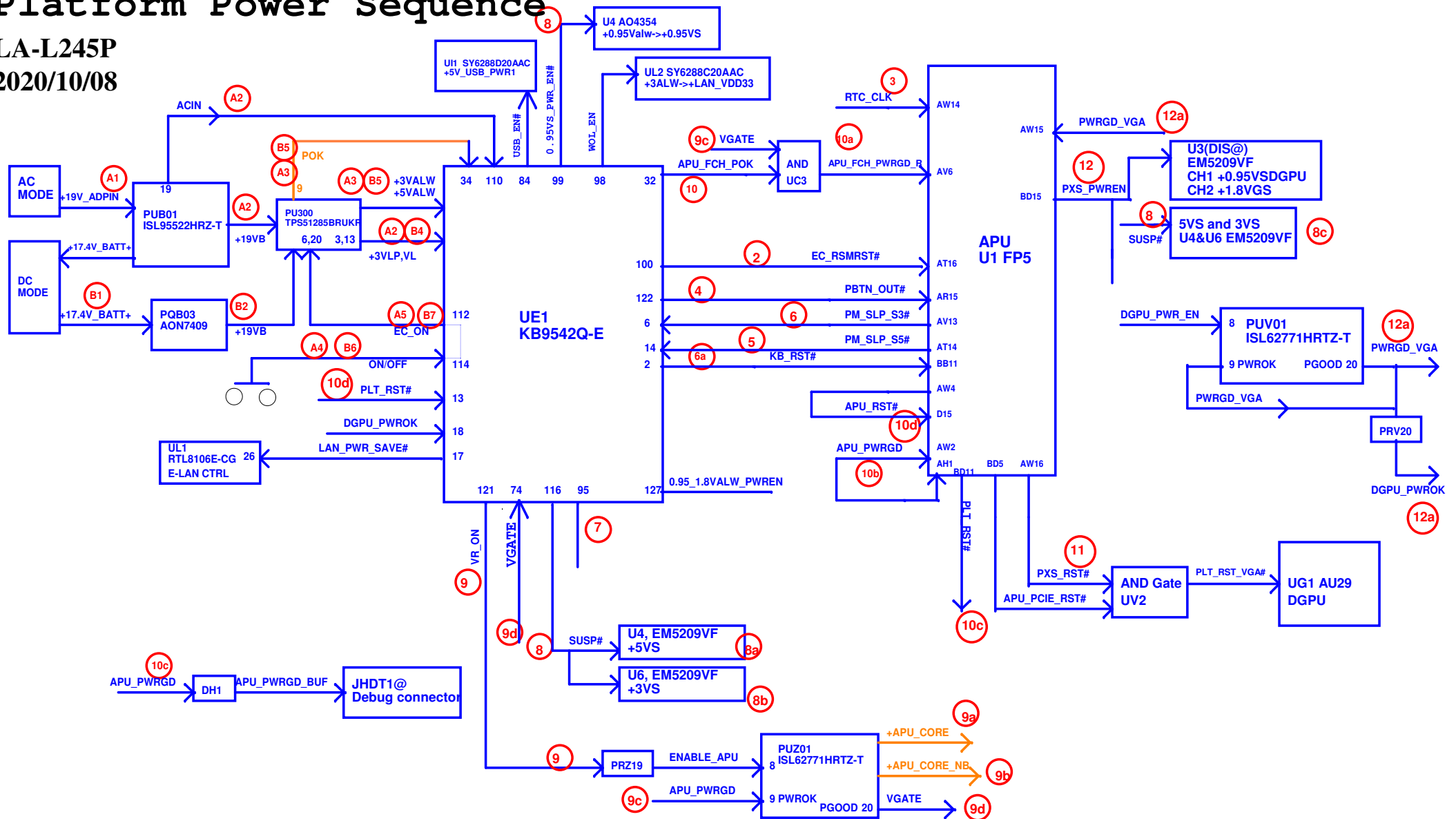
CPU PWR
Peripheral Device PWR



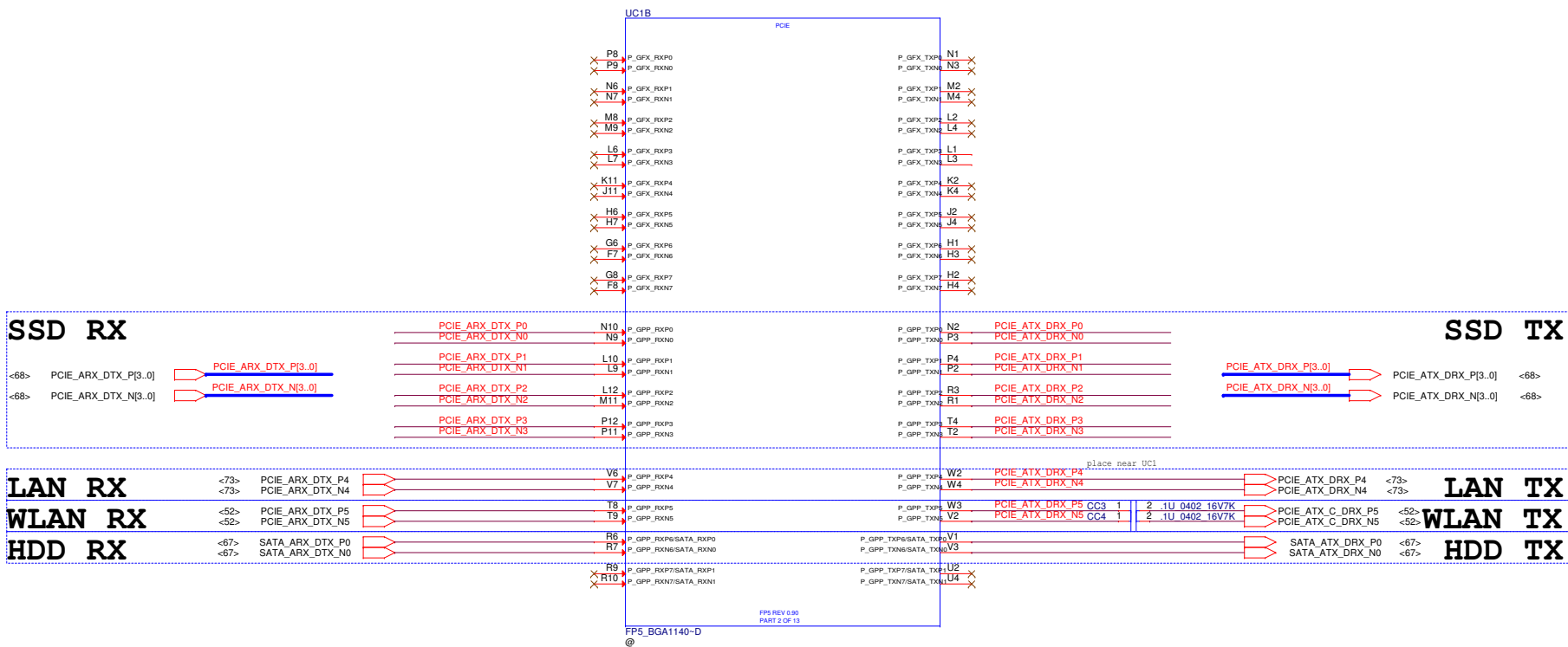
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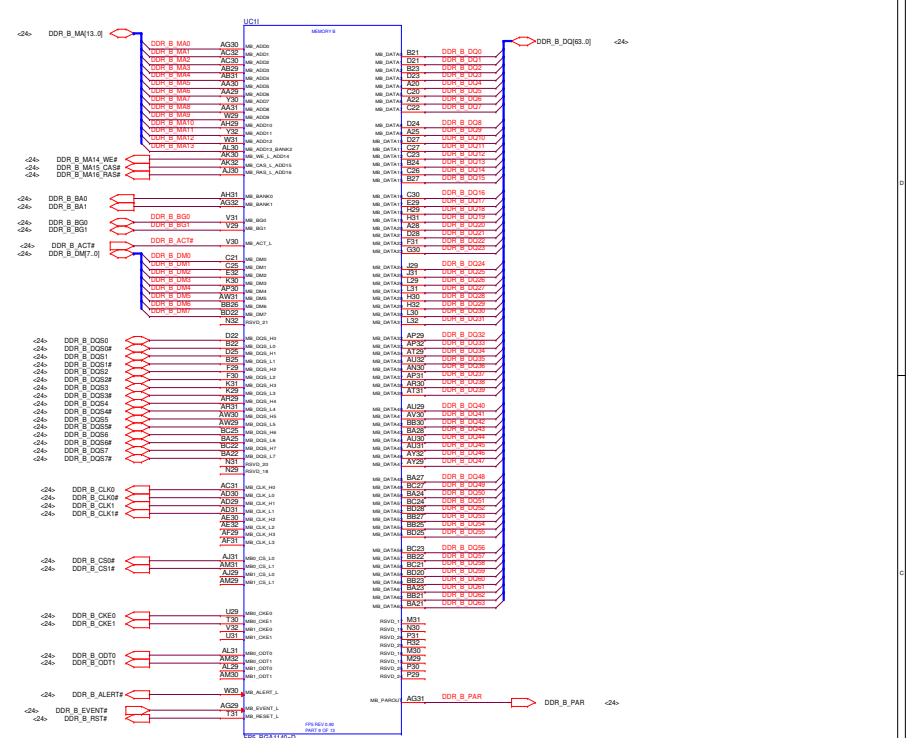
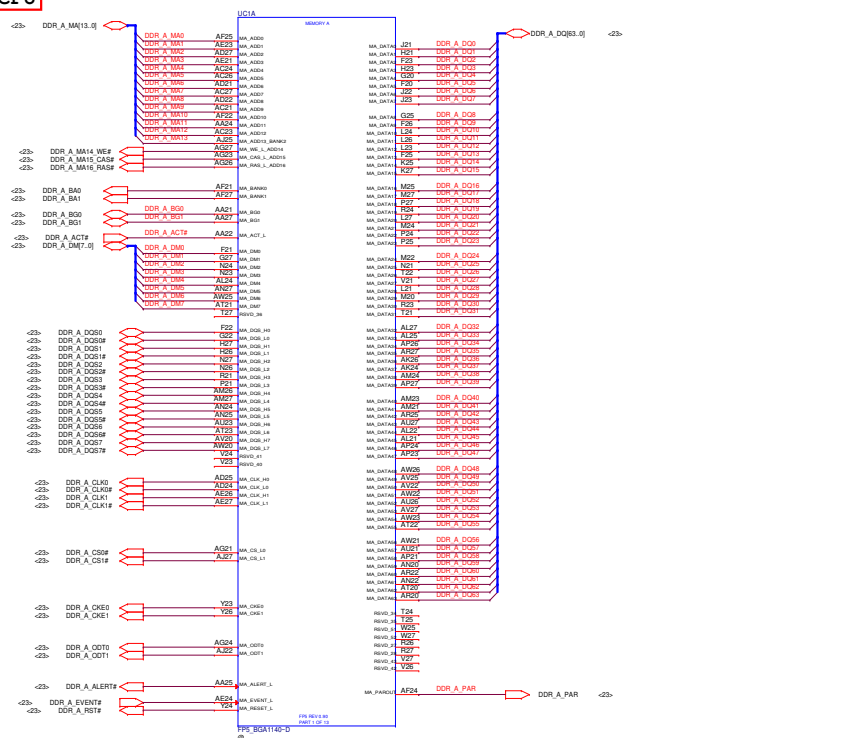
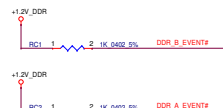
Platform Power Sequence

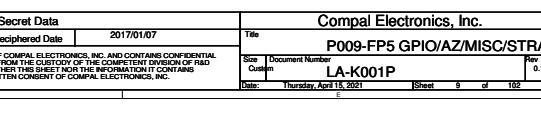
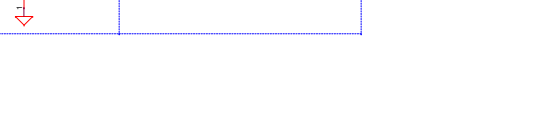
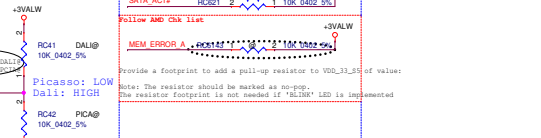
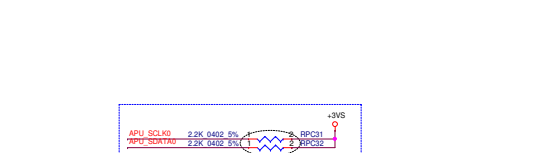
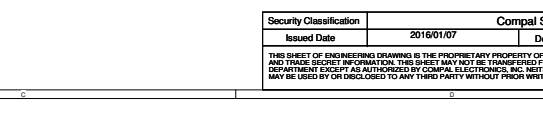
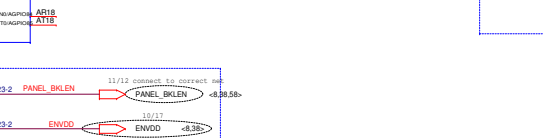
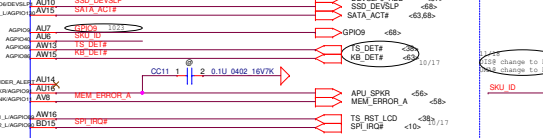
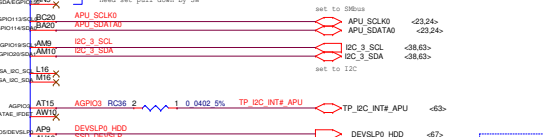
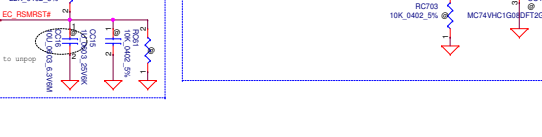
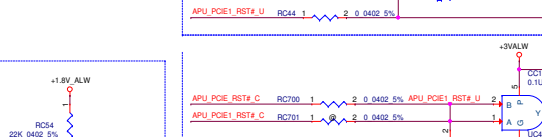
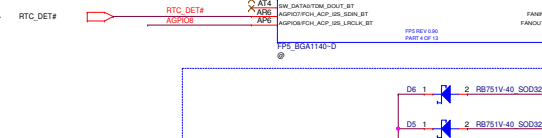
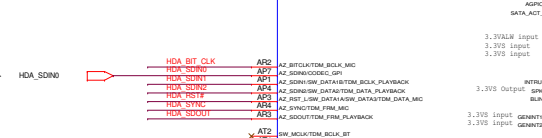
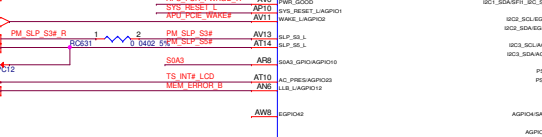
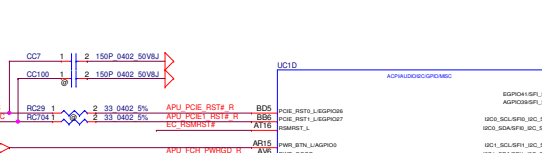
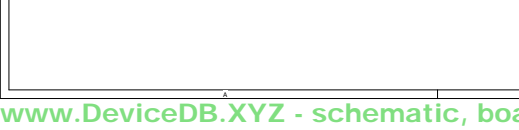
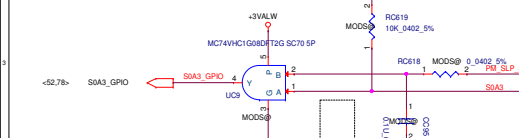
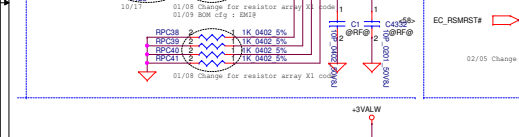
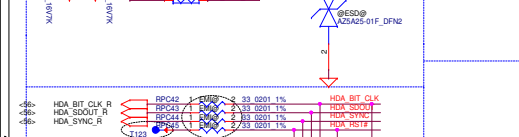
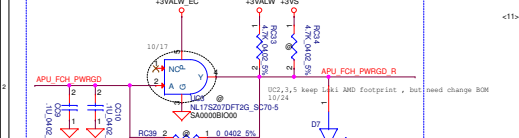
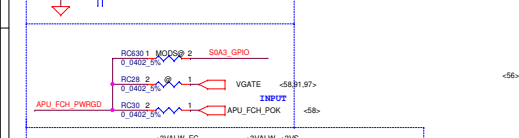
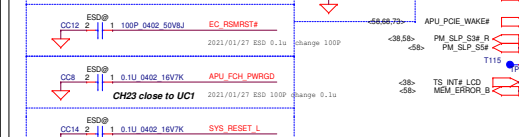
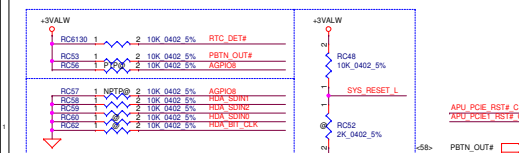
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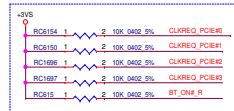




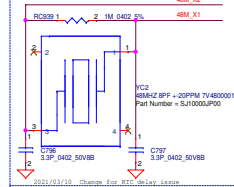


for Modern standby

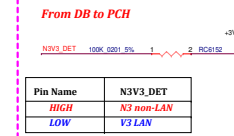
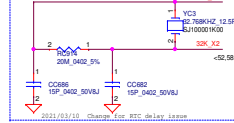
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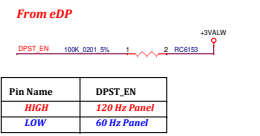
48MHz_CRYSTAL



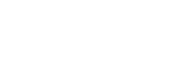
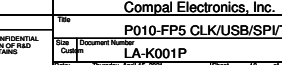
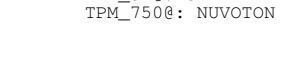
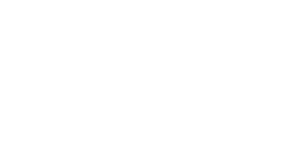
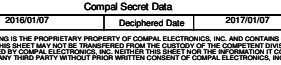
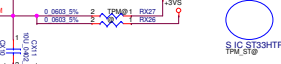
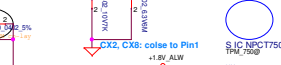
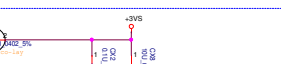
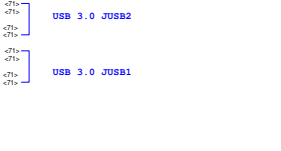
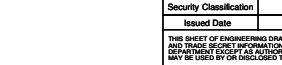
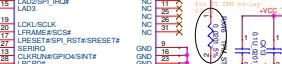
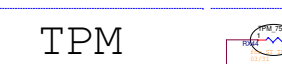
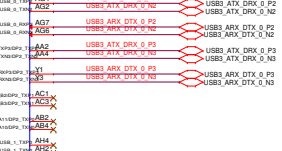
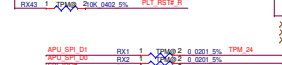
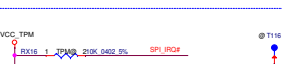
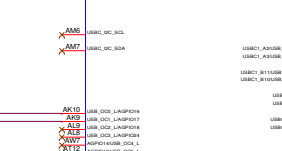
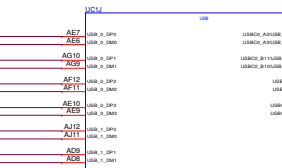
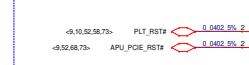
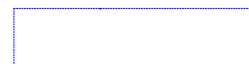
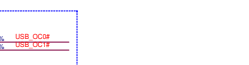
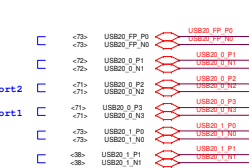
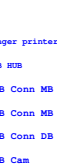
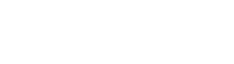
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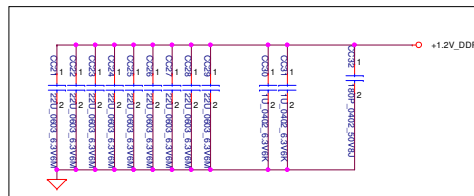


Pin Name	N3V3_DET
HIGH	N3 non-LAN
LOW	V3 LAN

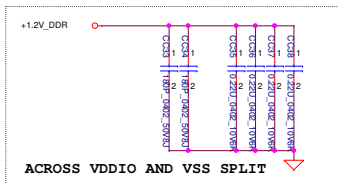


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HIGH	120 Hz Panel
LOW	60 Hz Panel

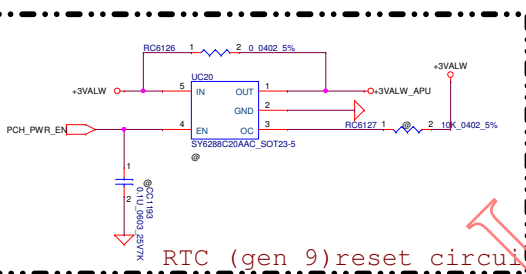
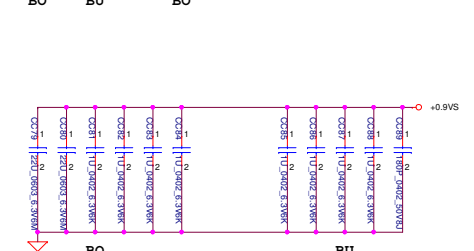
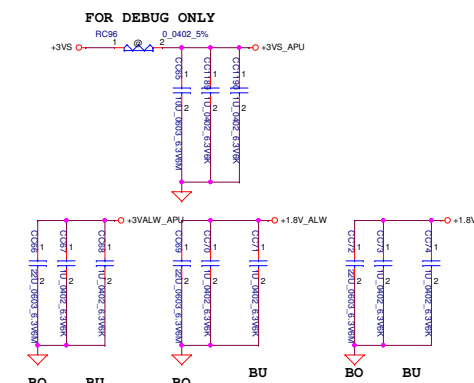




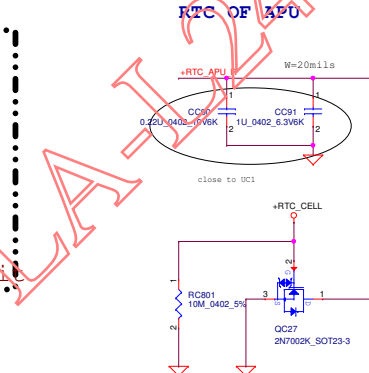
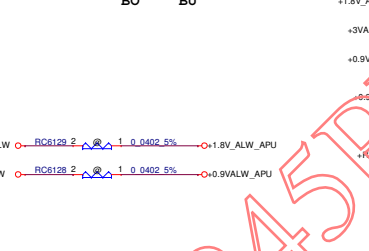
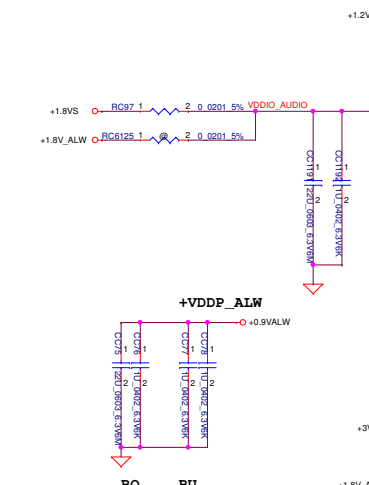
All BU(on bottom side under SOC)



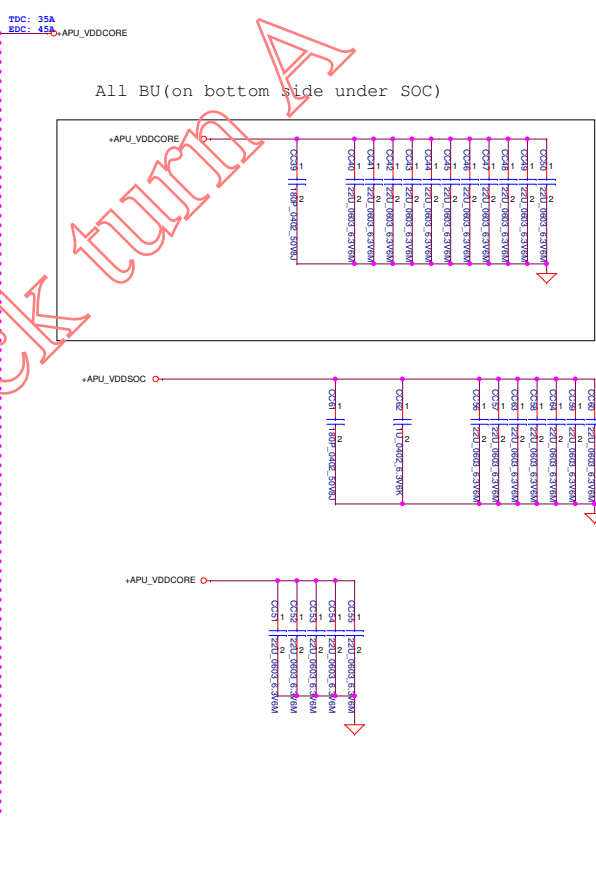
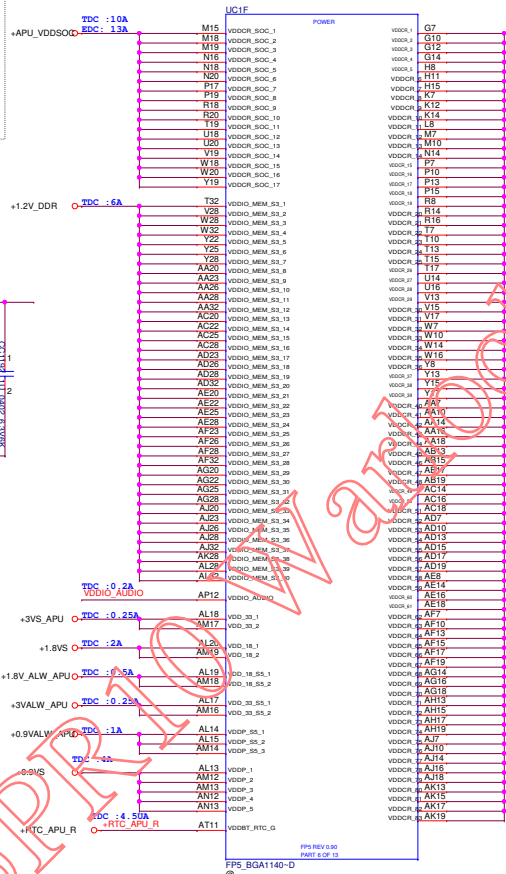
ACROSS VDDIO AND VSS SPLIT



RTC (gen 9) reset circuit



RTC OF APU



All BU(on bottom side under SOC)

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UC1G UC1H UC1K UC1M UC1L

FPS REV 0.90 PART 7 OF 13 FPS REV 0.90 PART 8 OF 13 FPS REV 0.90 PART 11 OF 13 FPS REV 0.90 PART 12 OF 13 FPS REV 0.90 PART 13 OF 13

FP5_BGA1140-D

CAMERAS

A18 CAM0_CSIG_CLOCKP B15 CAM0_CLK
C18 CAM0_CSIG_CLOCKN D15 CAM0_ICC_SCL
A15 CAM0_CSIG_DATA0 C14 CAM0_ICC_SDA
C15 CAM0_CSIG_DATA0 CAM0_SHUTDOWN
B16 CAM0_CSIG_DATAP1
C16 CAM0_CSIG_DATAN1
C19 CAM0_CSIG_DATA2
B18 CAM0_CSIG_DATA2
D17 CAM0_CSIG_DATA3
CAM0_CSIG_DATA3
D12 CAM1_CSIG_CLOCKP B10 CAM1_CLK
B12 CAM1_CSIG_CLOCKN A11 CAM1_ICC_SCL
C13 CAM1_CSIG_DATA0 C11 CAM1_ICC_SDA
A13 CAM1_CSIG_DATA0 CAM1_SHUTDOWN D11
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C12 CAM1_CSIG_DATAN1 CAM_IR_ILU D10
J13 RSVD_6

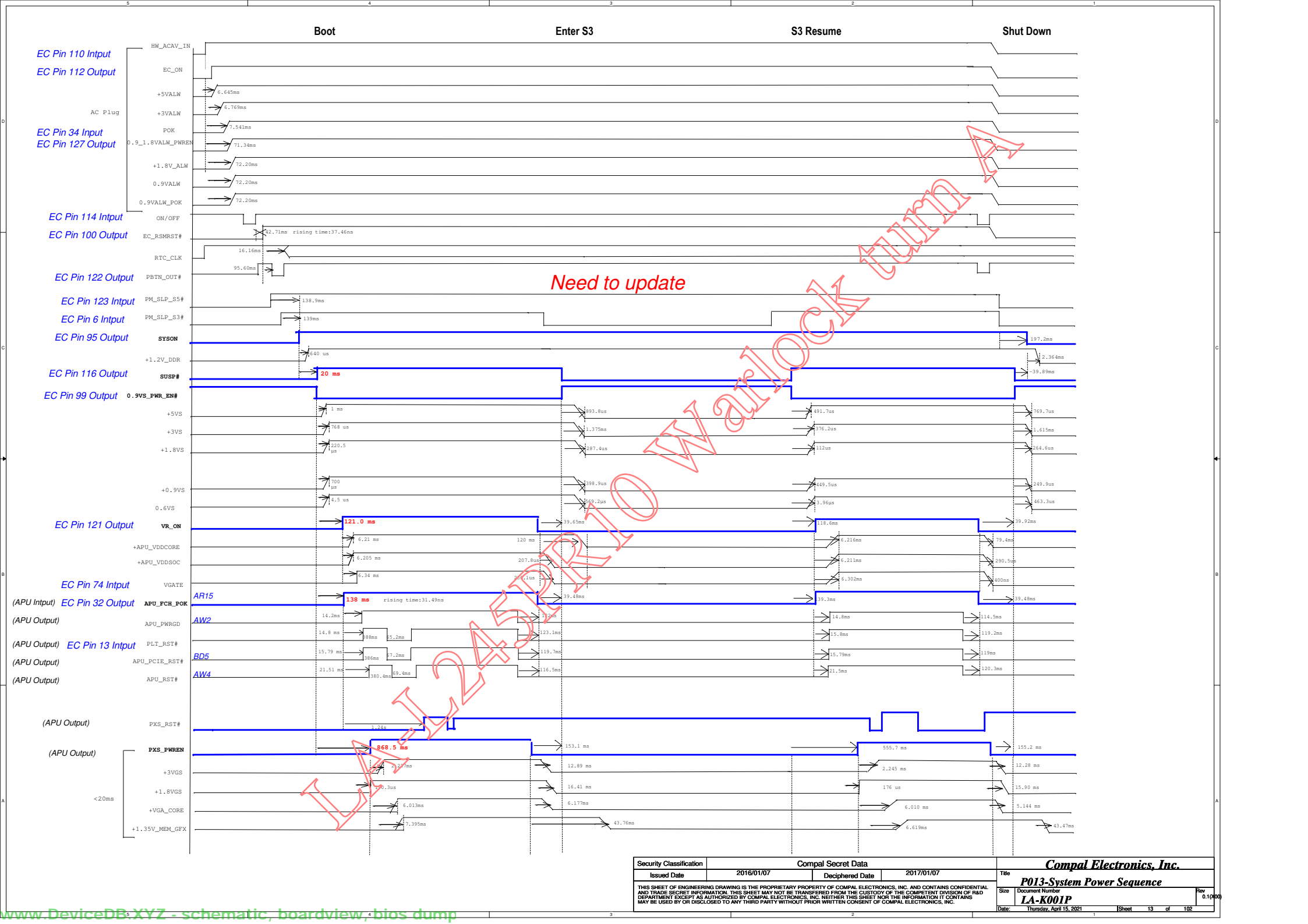
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www.DeviceDB.XYZ - schematic, boardview, bios dump

[illegible]



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CHA

Main Func = DIMM2



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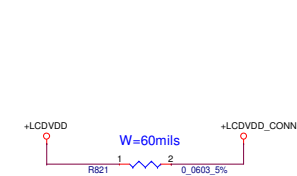
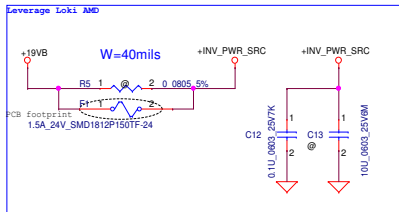
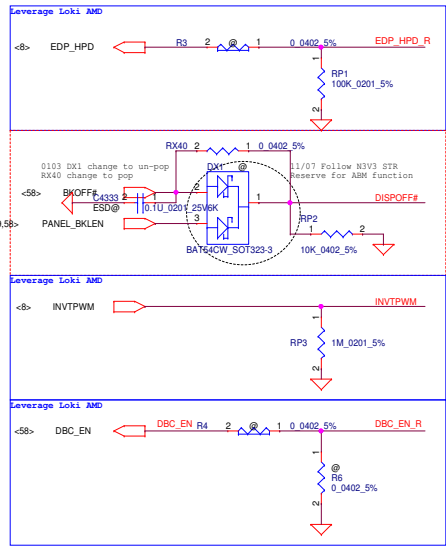
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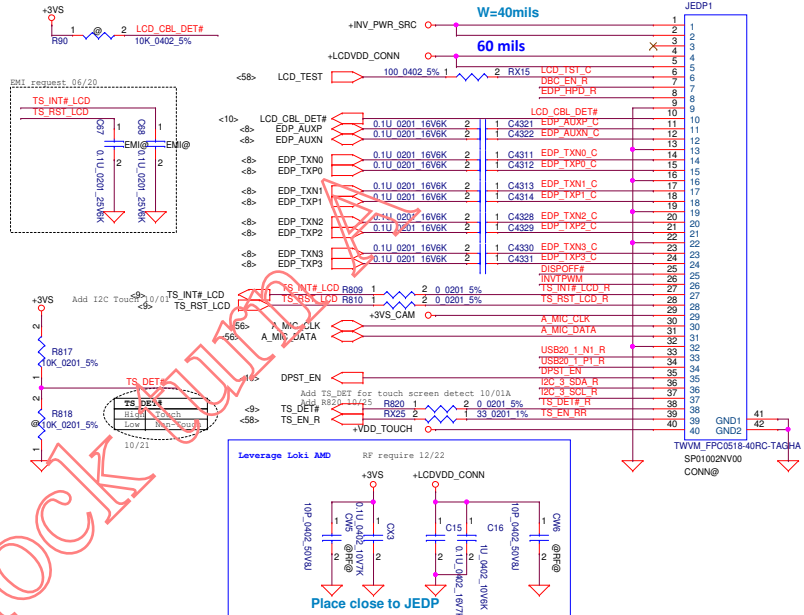
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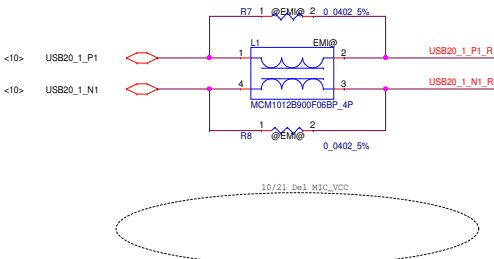
Main Func = LCD



10/20 Remove LCD power SW

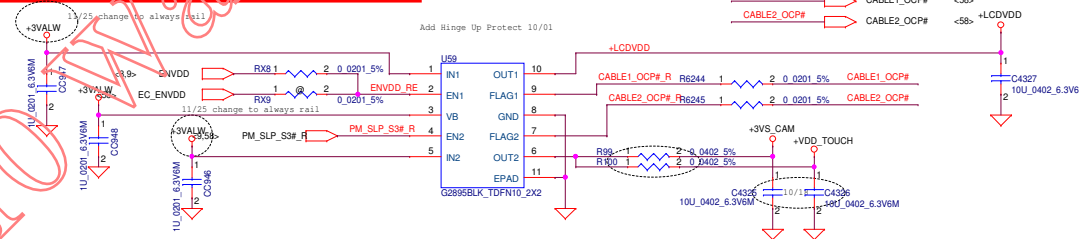


Main Func = Camera

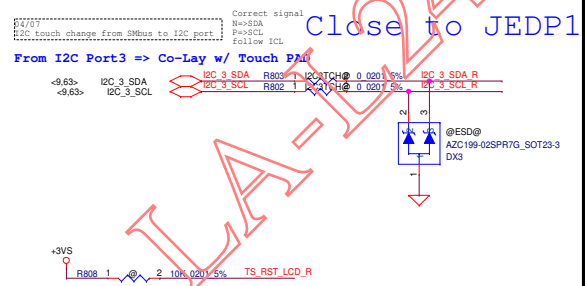


10/20 Remove Camera power

Main Func = Hinge Up Protect

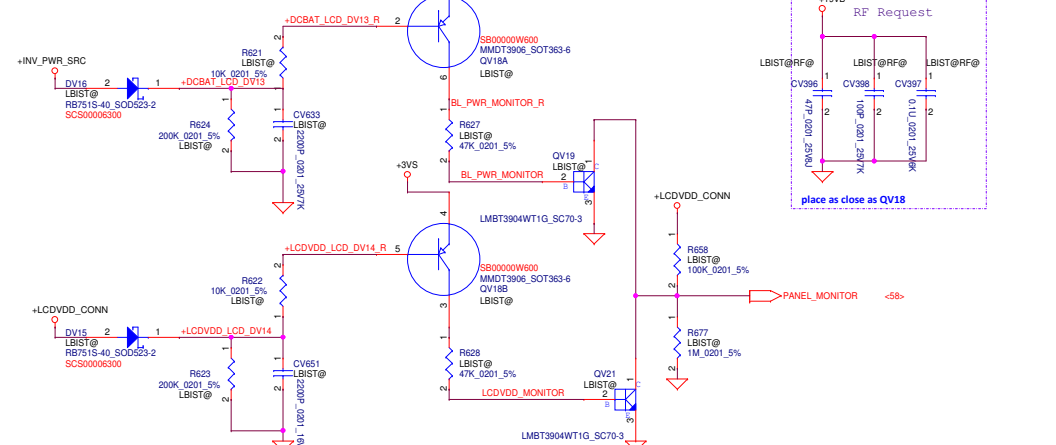


Main Func = Touch Screen



10/20 Remove Touch screen power

For BL_PWR_SRC & LCDVDD monitor

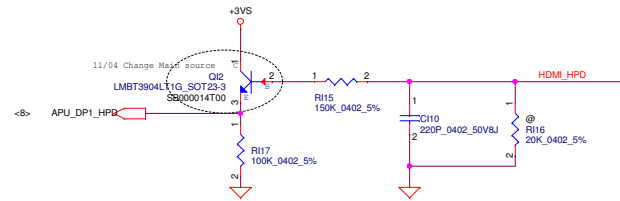
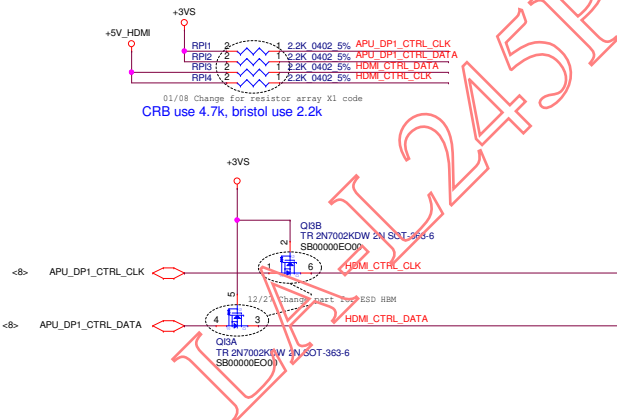
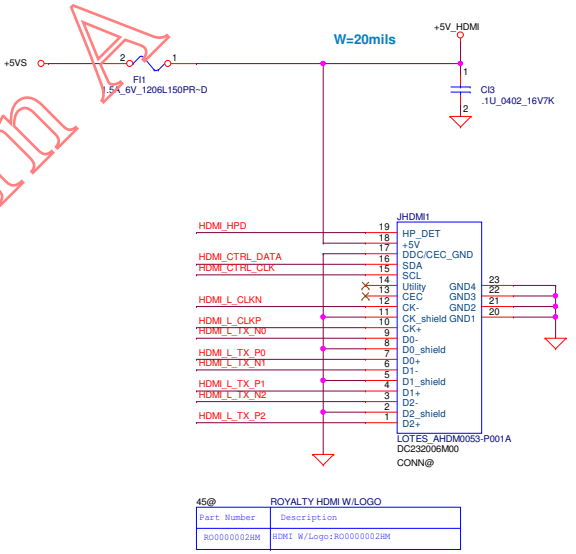
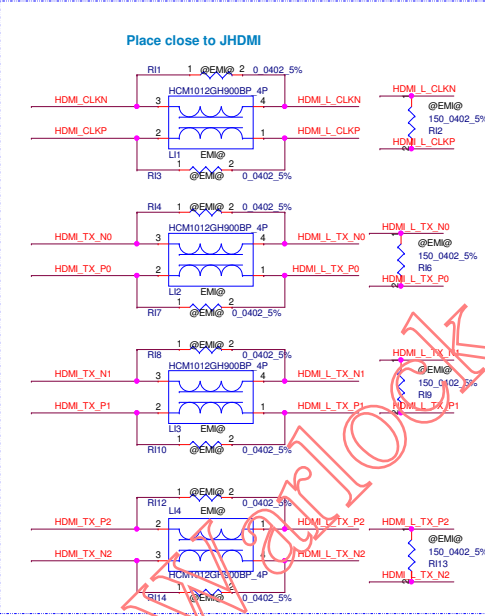
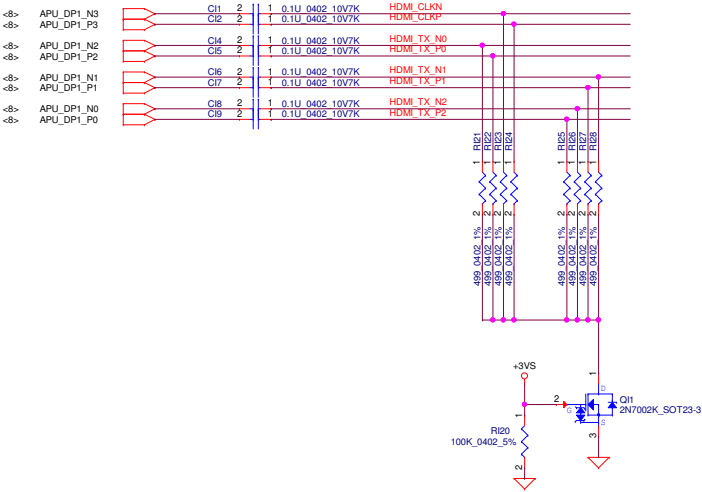


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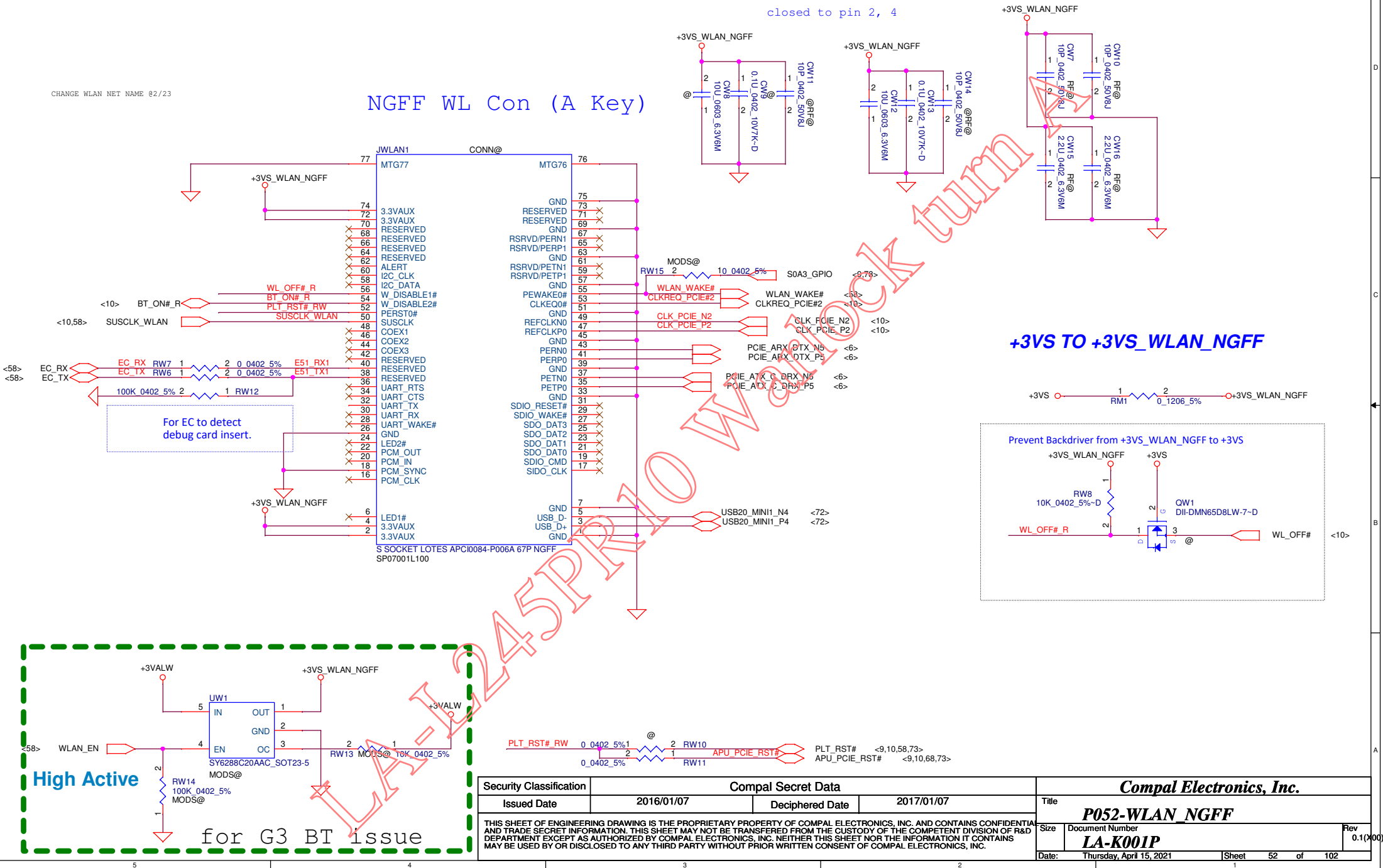
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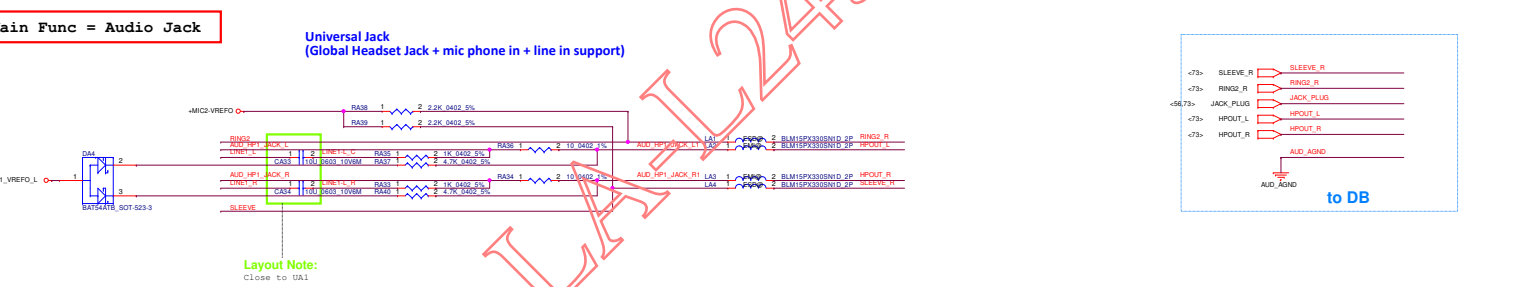
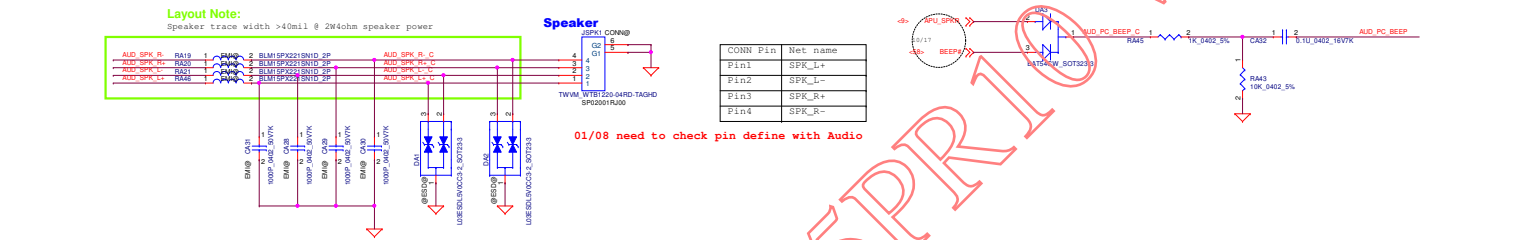
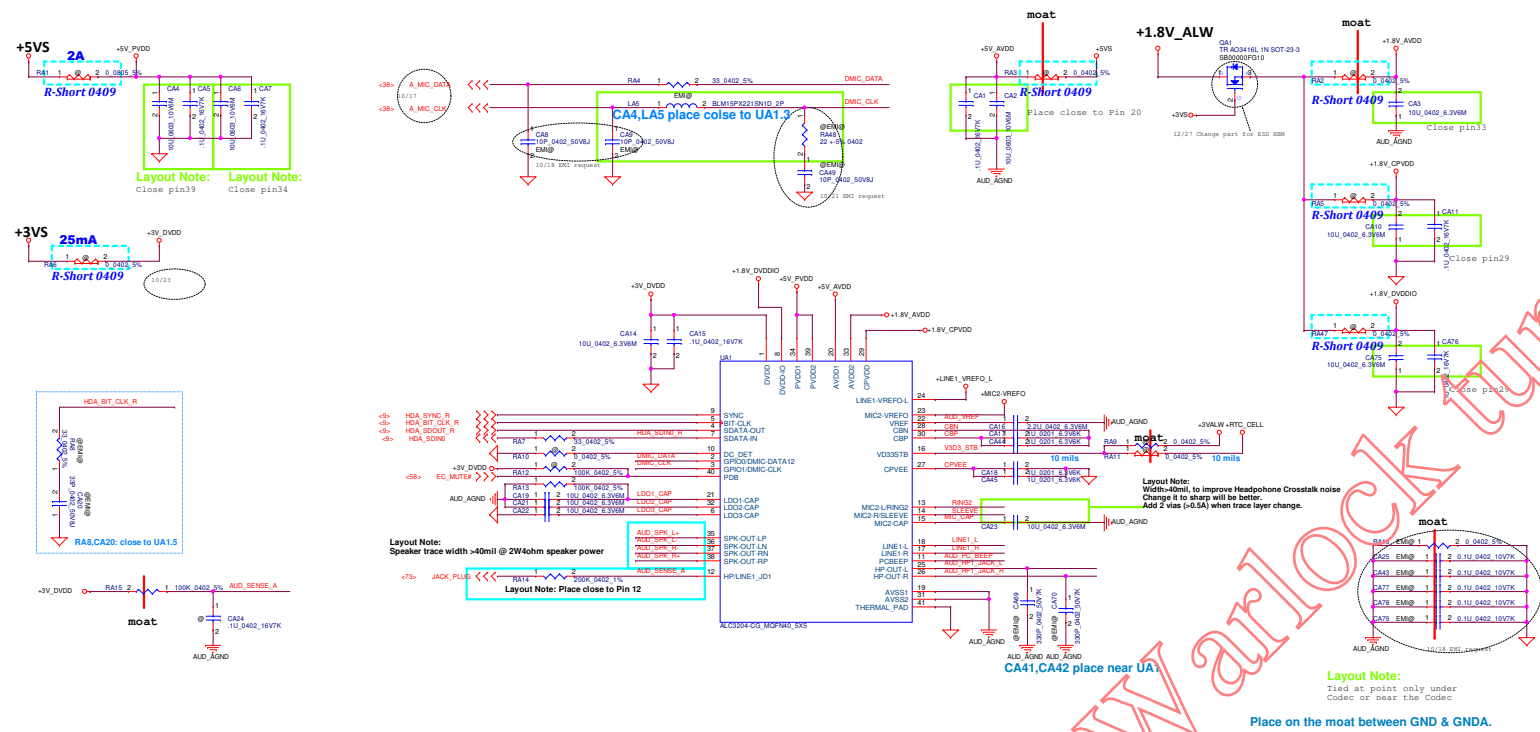
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www.DeviceDB.XYZ - schematic, boardview, bios dump

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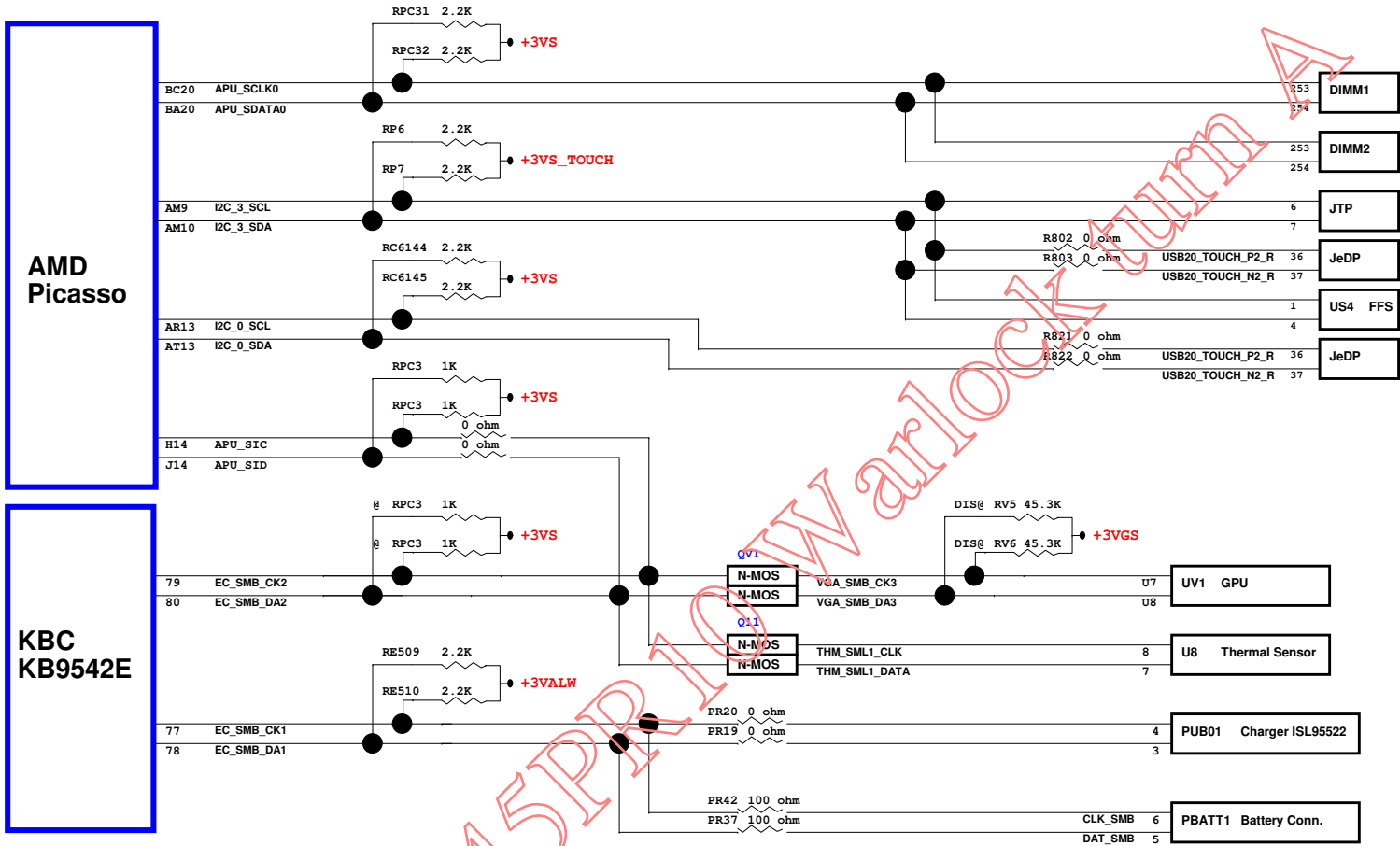
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		Size	Document Number	0.1(200)	
		C	LA-K001P		
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Reserve

LA-L245PR10 Warlock turn A

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				C	LA-K001P
				Date:	Thursday, April 15, 2021
				Sheet	62 of 102
				Rev	0.1(200)

Reserve

LA-L245PR10 Warlock turn A

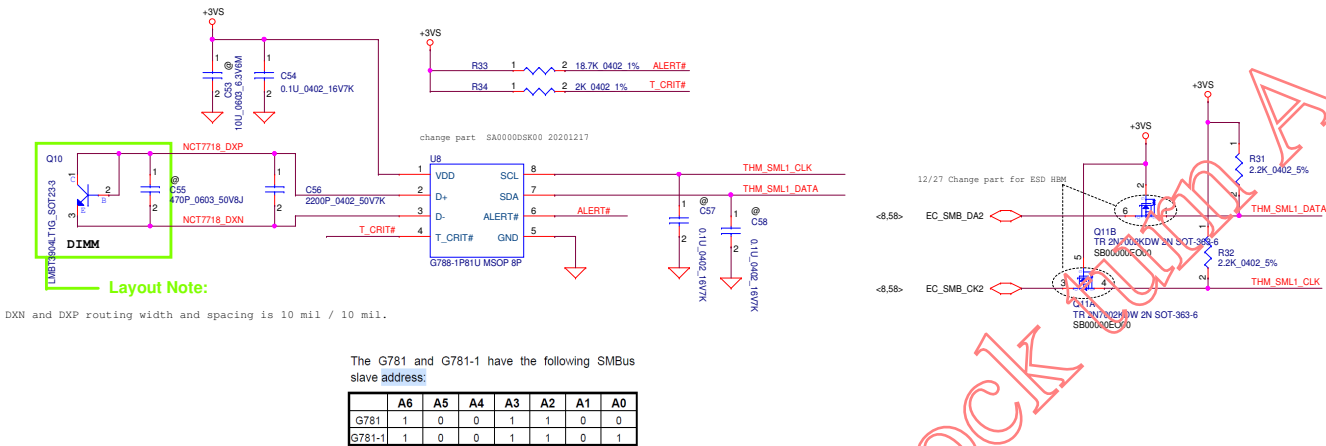
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date		2016/01/07	Deciphered Date	2017/01/07	Title
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		C	LA-K001P		
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LA-L245PR10 Warlock turn A

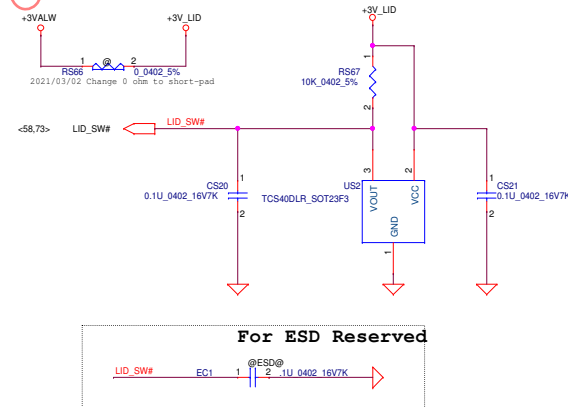
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Issued Date		2016/01/07	Deciphered Date	2017/01/07	Title
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		Size	Document Number	0.1(200)	
		C	LA-K001P		
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Main Func = Thermal

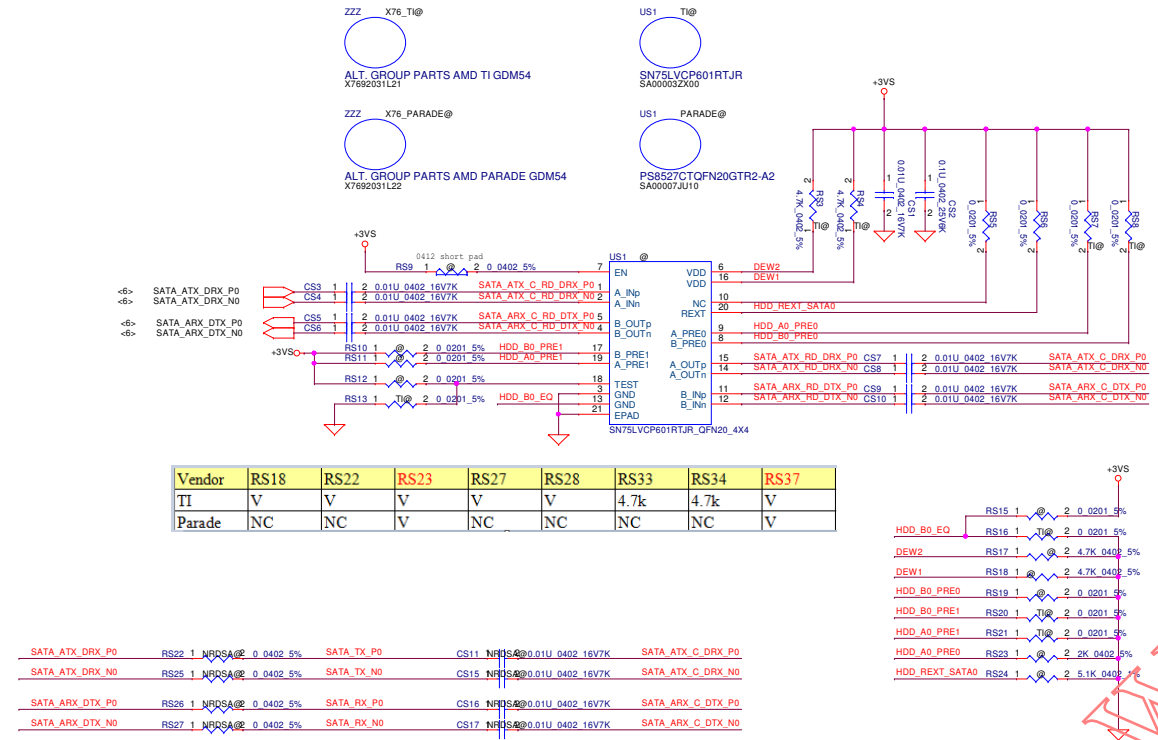


Main Func = Finger Printer

Main Func = Hall sensor



Main Func = HDD



+5V_HDD Source
60 mils
SHORT

Main Func = FFS

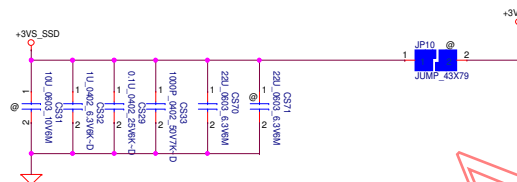
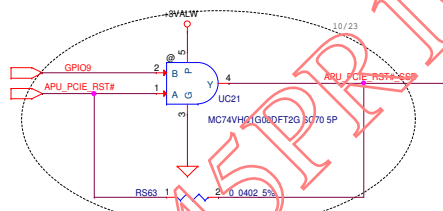
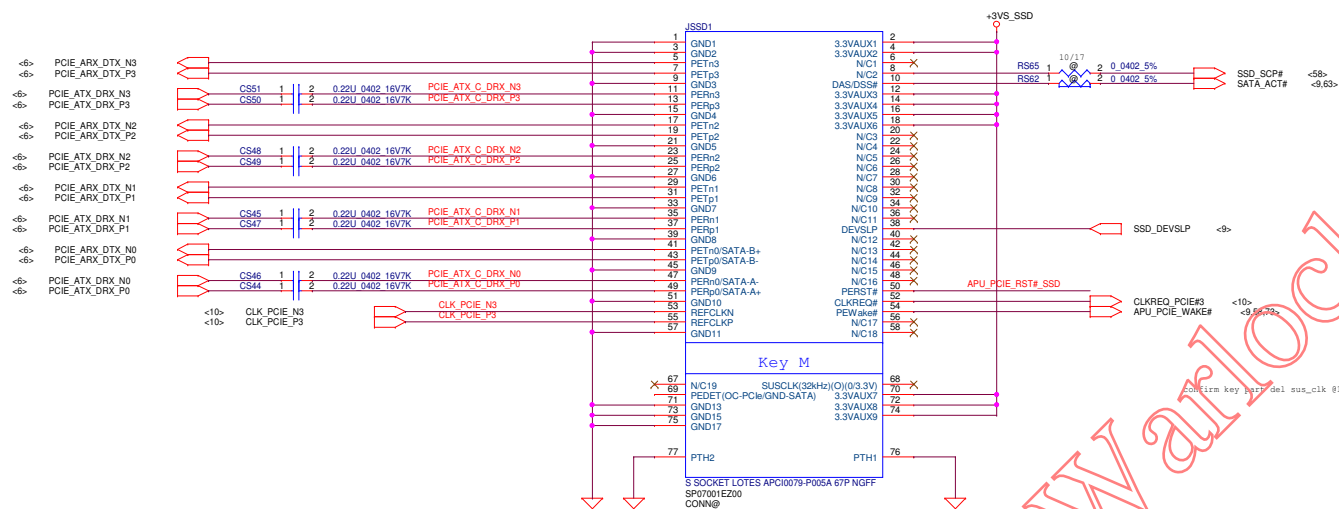
Main Func = ODD

10/20 no support function in FFS

10/12 no support function in ODD

Main Func = SSD

NGFF Key M



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Size C	Document Number	LA-K001P		Date:	Thursday, April 15, 2021
		Sheet	68	of	102

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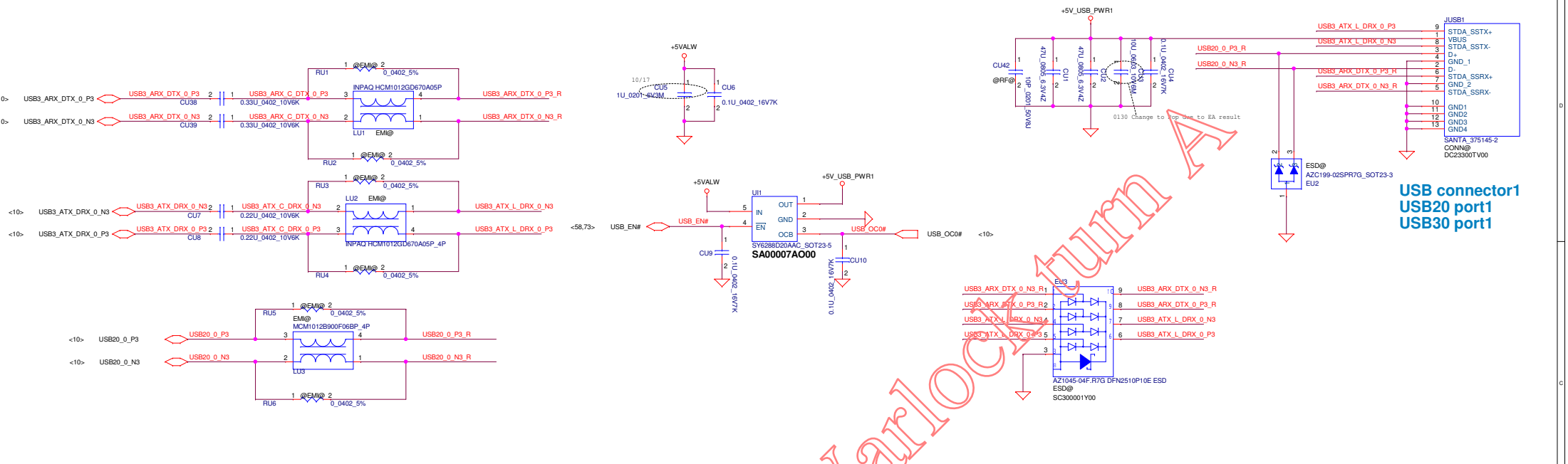
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date		2016/01/07	Deciphered Date	2017/01/07	Title
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		Size	Document Number	0.1(200)	
		C	LA-K001P		
		Date:	Thursday, April 15, 2021	Sheet	69 of 102

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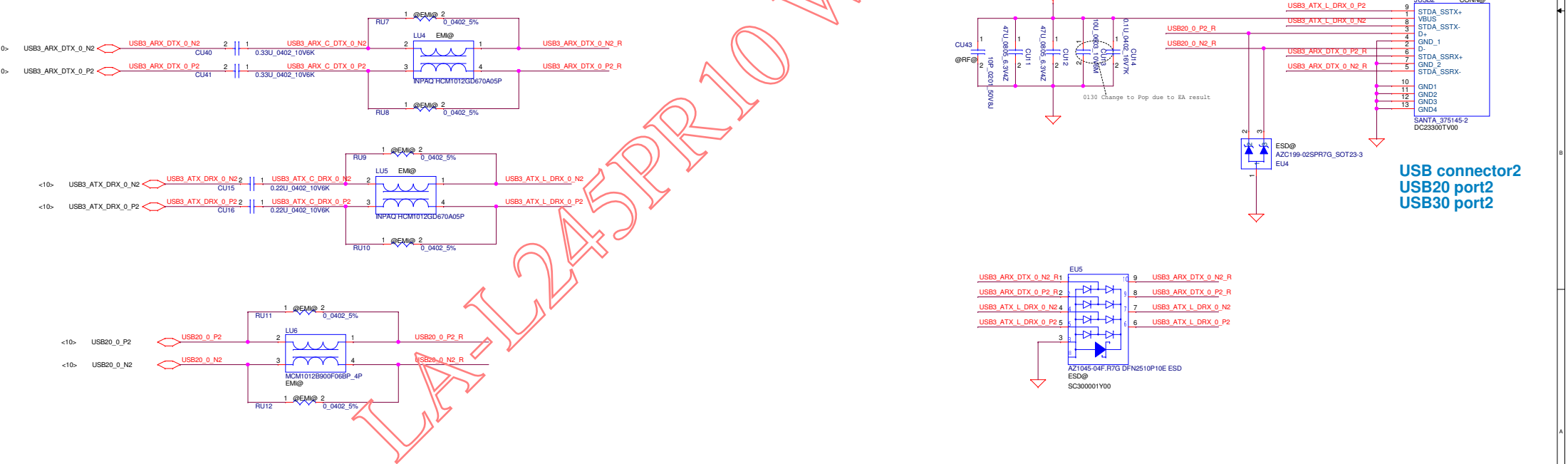
LA-L245PR10 Warlock turn A

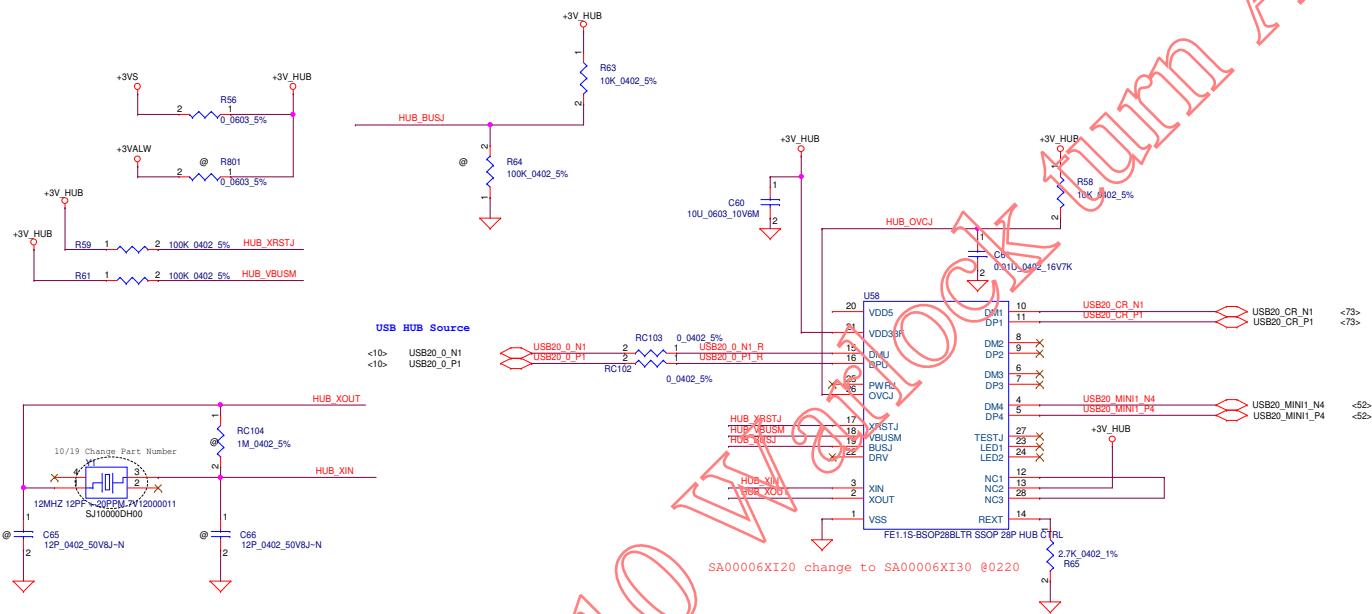
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Issued Date		2016/01/07	Deciphered Date	2017/01/07	Title
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		Size	Document Number	0.1(200)	
		C	LA-K001P		
		Date:	Thursday, April 15, 2021	Sheet	70 of 102

Main Func = USB3.0 Port1



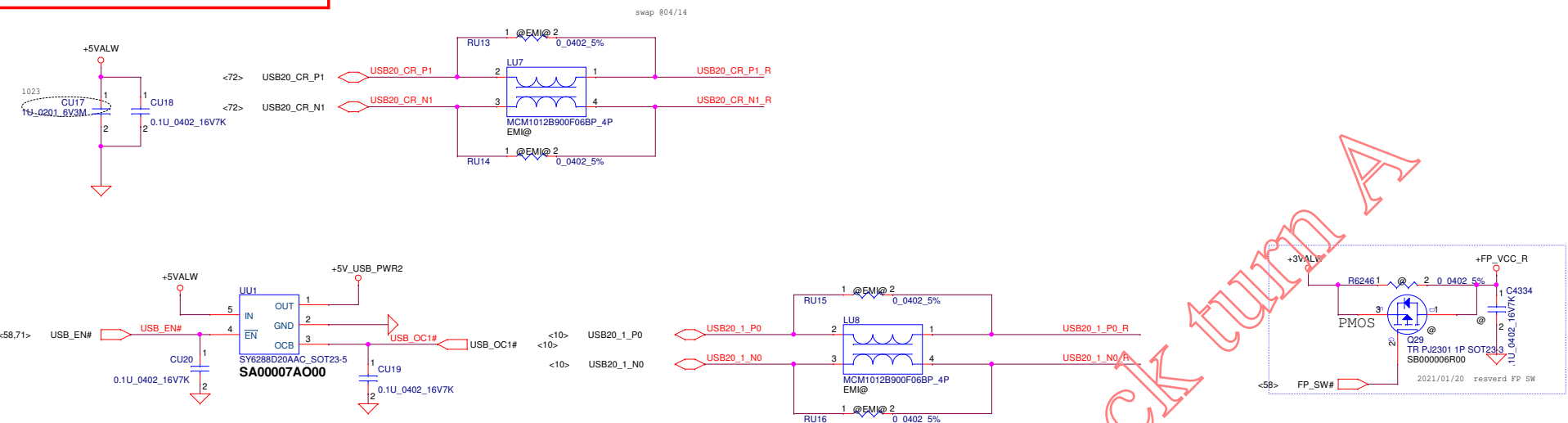
Main Func = USB3.0 Port2



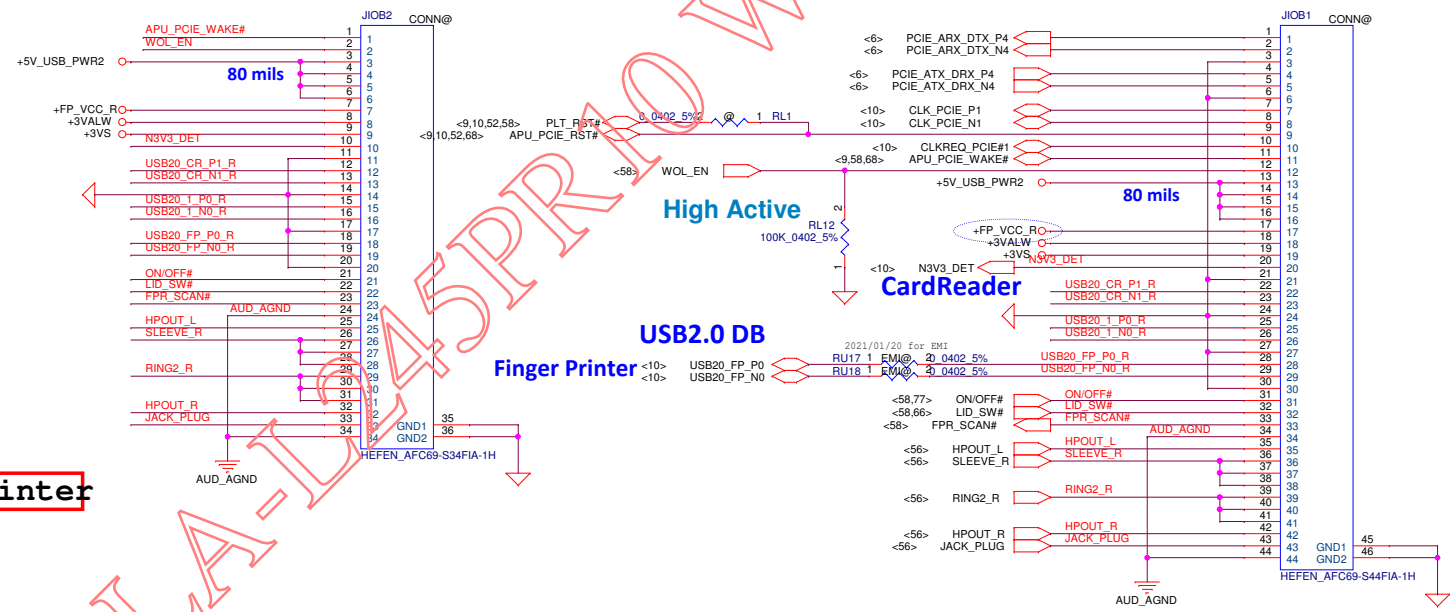


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Size	C	Document Number	LA-K001P	Rev
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Main Func = IO Connector



JIOB1 and JIOB2 CONN co-lay



Main Func = Finger Printer



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Issued Date	2016/01/07	Deciphered Date	2017/01/07	P073-USB2.0 IO(DB)	
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				LA-K001P	0.1(00)
				Date	Thursday, April 15, 2021
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		Size	Document Number	0.1(200)	
		C	LA-K001P		
		Date:	Thursday, April 15, 2021	Sheet	74 of 102

Main Func = Reserve

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		Size	Document Number	0.1(200)	
		C	LA-K001P		
		Date:	Thursday, April 15, 2021	Sheet	75 of 102

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		C	LA-K001P		
		Date:	Thursday, April 15, 2021	Sheet	76 of 102

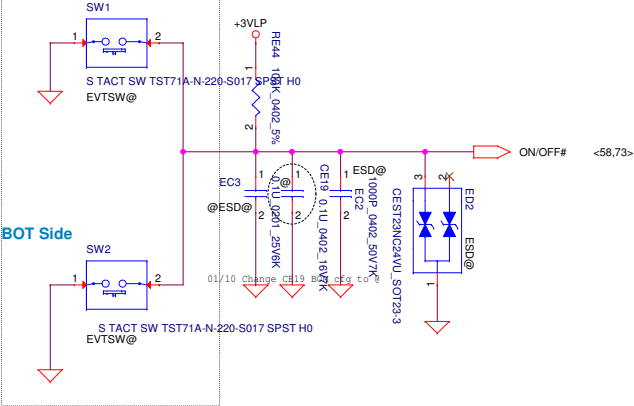
Main Func = Power Switch

Power button

Pop only before MP

ON/OFF switch

TOP Side



Main Func = PCB PN

Warlock LA-L245P PCB

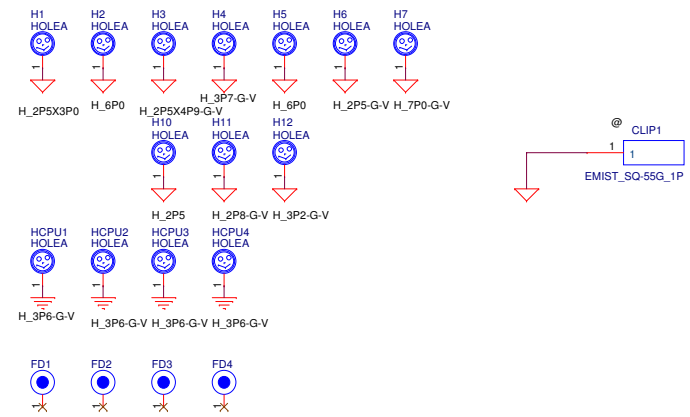
Part Number	Description	
DA6002E3000	PCB 3LI LA-L245P REV0 M/B 1 S	N3
PCB_N3@		
Part Number	Description	
DAZ3LI00100	PCB GDM54 LA-L245P LS-L241P 02	DAZ R1
PCB_R1_N3@		
Part Number	Description	
DAZ3LI00101	PCB GDM54 LA-L245P LS-L241P 02 GOLD A31 !	DAZ R3
PCB_R3G_V3@		
Part Number	Description	
DAZ3LI00102	PCB GDM54 LA-L245P LS-L241P 02 TRIPOD A31 !	
@PCB_R3T_N3@		
Part Number	Description	
DAZ3LI00103	PCB GDM54 LA-L245P LS-L241P 02 HANNSTAR A31 !	
@PCB_R3H_N3@		
Part Number	Description	
DAZ3LI00104	PCB GDM54 LA-L245P LS-L241P 02 T-MAC A31 !	
@PCB_R3TR_N3@		

Part Number	Description	
DA6002E3100	PCB 3LI LA-L245P REV0 M/B 1 L S	V3
PCB_V3@		
Part Number	Description	
DAZ3LN00100	PCB GDM5D LA-L245P LS-L242P 02	DAZ R1
PCB_R1_V3@		
Part Number	Description	
DAZ3LN00101	PCB GDM5D LA-L245P LS-L242P 02 GOLD A31 !	DAZ R3
PCB_R3G_V3@		
Part Number	Description	
DAZ3LN00102	PCB GDM5D LA-L245P LS-L242P 02 TRIPOD A31 !	
@PCB_R3T_V3@		
Part Number	Description	
DAZ3LN00103	PCB GDM5D LA-L245P LS-L242P 02 HANNSTAR A31 !	
@PCB_R3H_V3@		
Part Number	Description	
DAZ3LN00104	PCB GDM5D LA-L245P LS-L242P 02 T-MAC A31 !	
@PCB_R3TR_V3@		

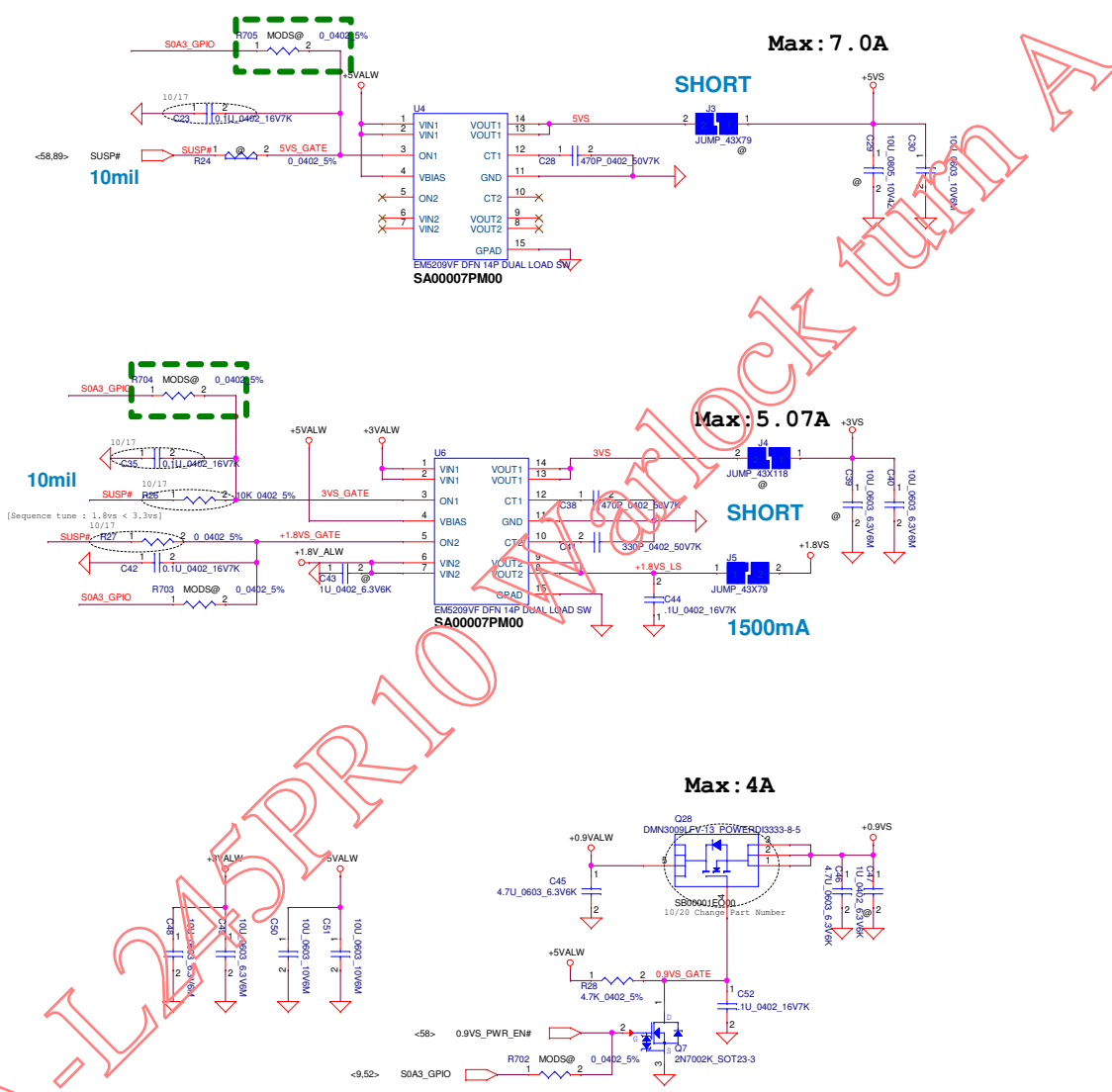
Main Func = FAN

Main Func = Screw Hole

Screw hole/FD



+5VS and +3VS switch



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		C	LA-K001P		
		Date:	Thursday, April 15, 2021	Sheet	79 of 102

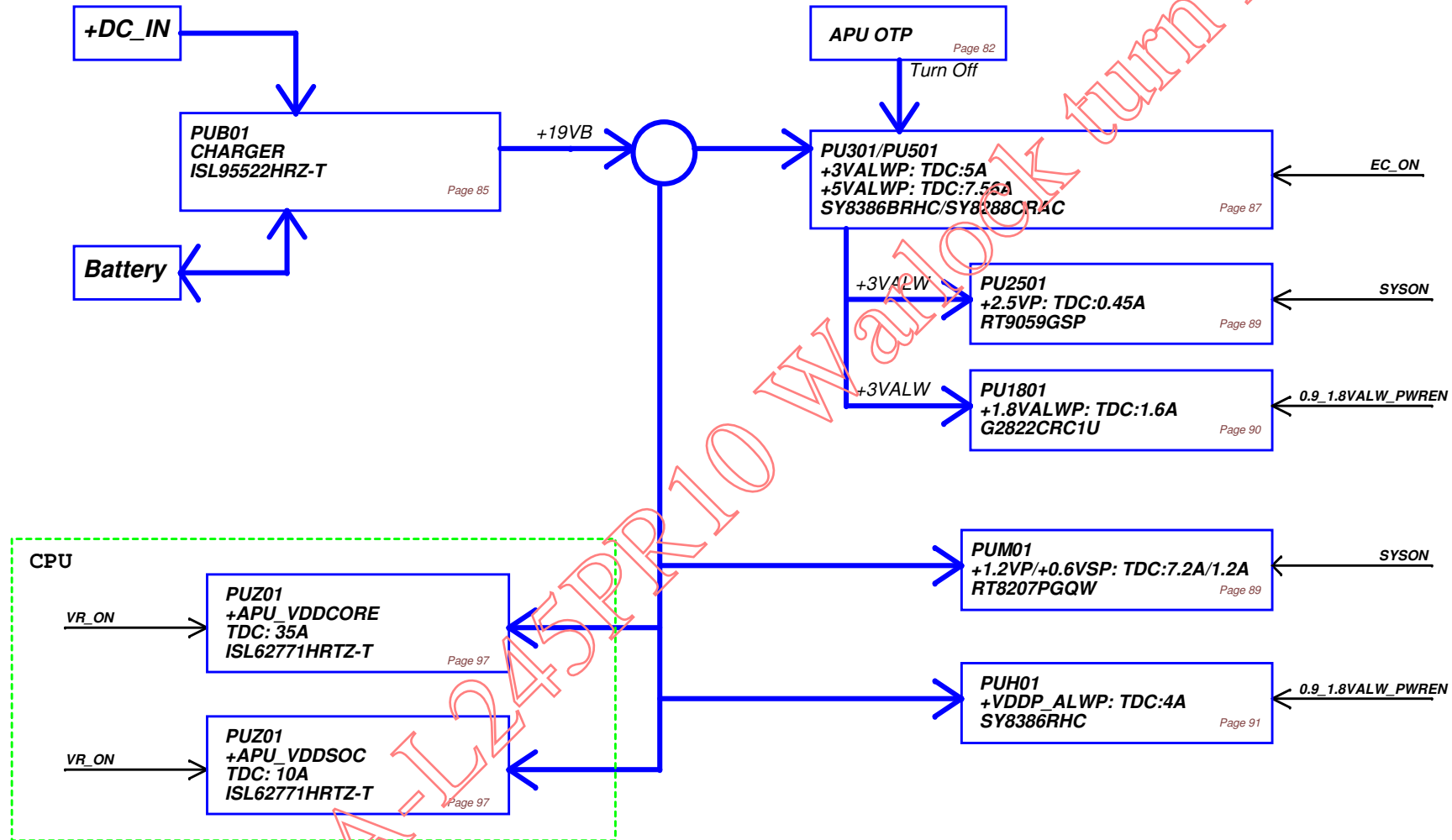
Main Func = Reserve

Reserve

LA-L245PR10 Warlock turn A

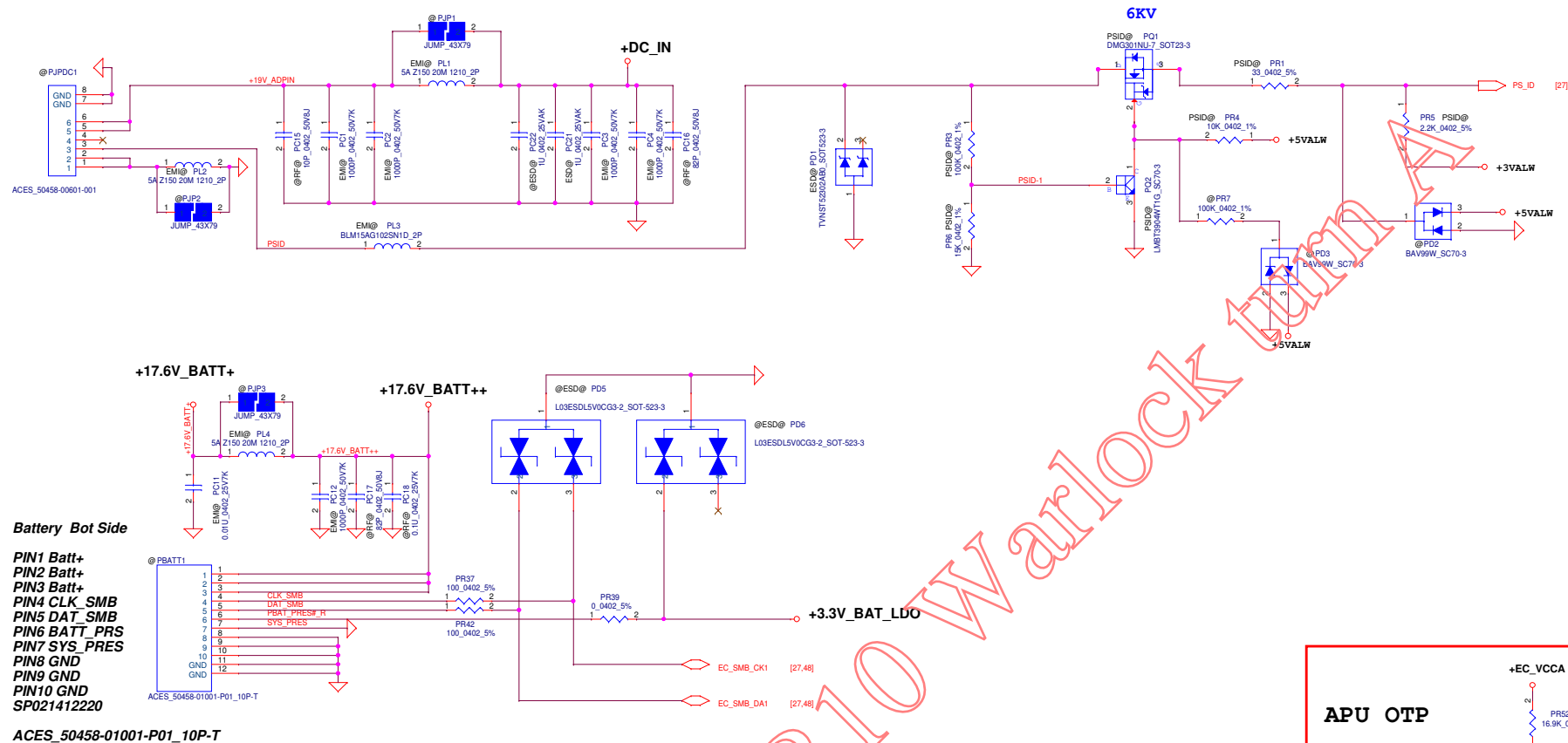
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		Size	Document Number	0.1(200)	
		C	LA-K001P		
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Power Block Diagram



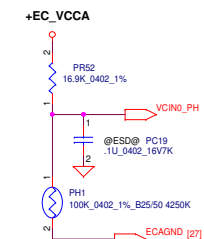
Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2020/10/08	Deciphered Date	2020/07/20	Title	PWR Power Block Diagram
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Main Func = DC-IN/BATT CONN/RTC/OTP



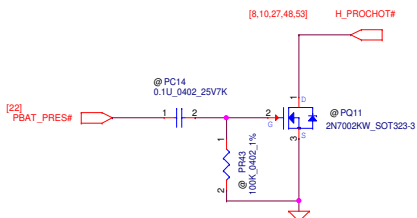
APU OTP

PH1 under CPU bottom side :
CPU thermal protection
Trigger=1V
92 +/- 3 degree C
Recover=2.19V
50 +/- 3 degree C



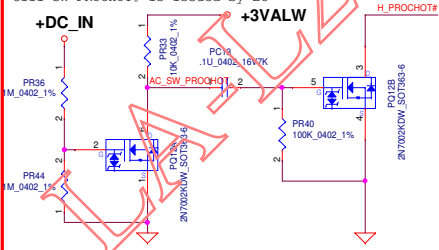
Adapter protection:

if battery removed, adaptor only,
then trigger the H_PROCHOT#,
keep @ in BOM since battery can not
be removed by end user

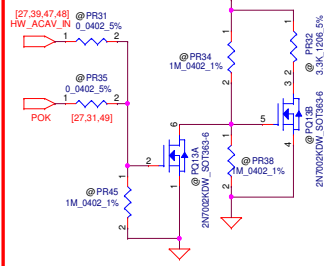


Battery protection:

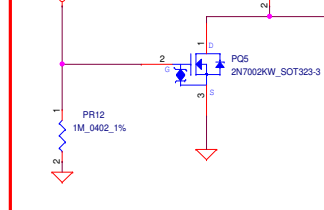
asserts H_PROCHOT# when adaptor is
unplugged, keep low for 10ms
till SW_PROCHOT# is issued by EC



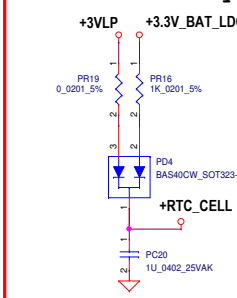
Erp Iot6 Circuit



+3V_BAT_LDO



COIN RTC Battery



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				Sheet	82 of 121

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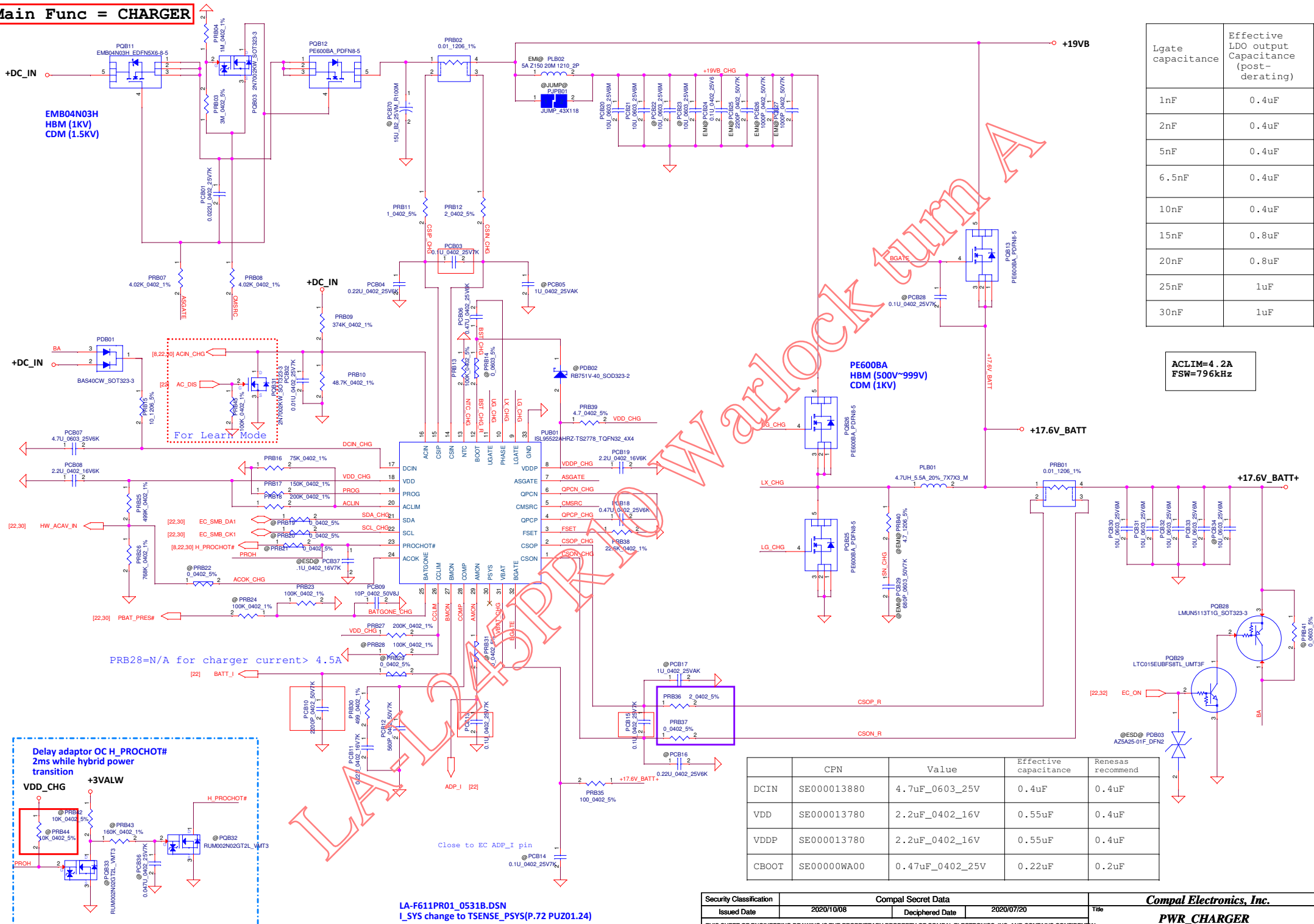
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Issued Date	2020/10/08	Deciphered Date	2020/07/20	Title		
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					Document Number
					LA-L245P
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					X00
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Main Func = CHARGER



Lgate capacitance	Effective LDO output Capacitance (post-derating)
1nF	0.4uF
2nF	0.4uF
5nF	0.4uF
6.5nF	0.4uF
10nF	0.4uF
15nF	0.8uF
20nF	0.8uF
25nF	1uF
30nF	1uF

ACLIM=4.2A
FSW=796kHz

	CPN	Value	Effective capacitance	Renesas recommend
DCIN	SE000013880	4.7uF_0603_25V	0.4uF	0.4uF
VDD	SE000013780	2.2uF_0402_16V	0.55uF	0.4uF
VDDP	SE000013780	2.2uF_0402_16V	0.55uF	0.4uF
CBOOT	SE00000WA00	0.47uF_0402_25V	0.22uF	0.2uF

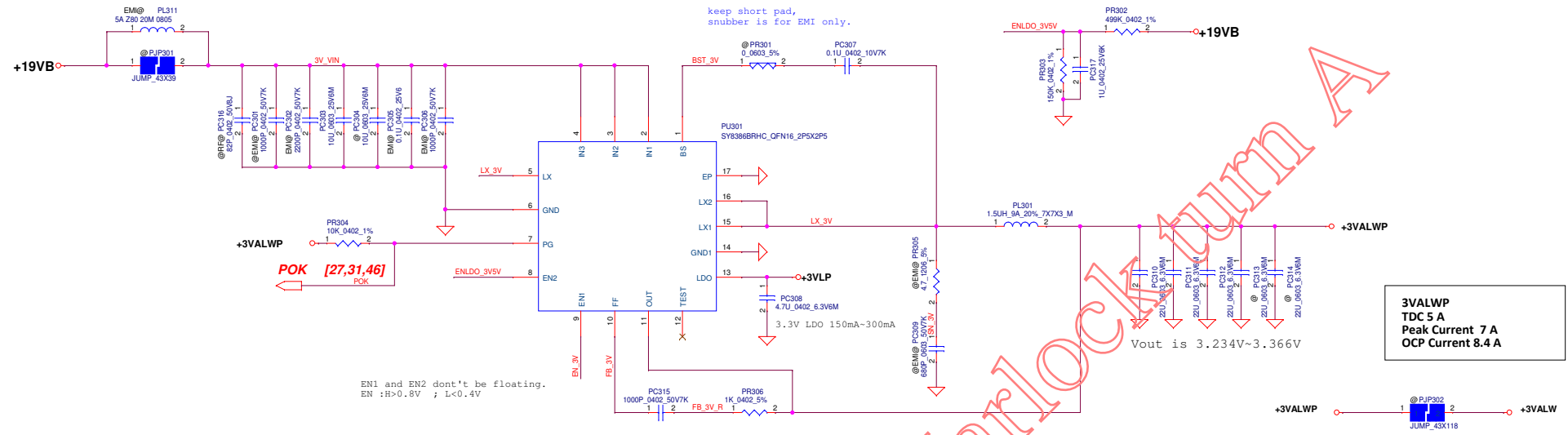
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2020/10/08	Deciphered Date	2020/07/20	Title	PWR CHARGER	
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				Date	Thursday April 15 2021	[Sheet 85 of 121]

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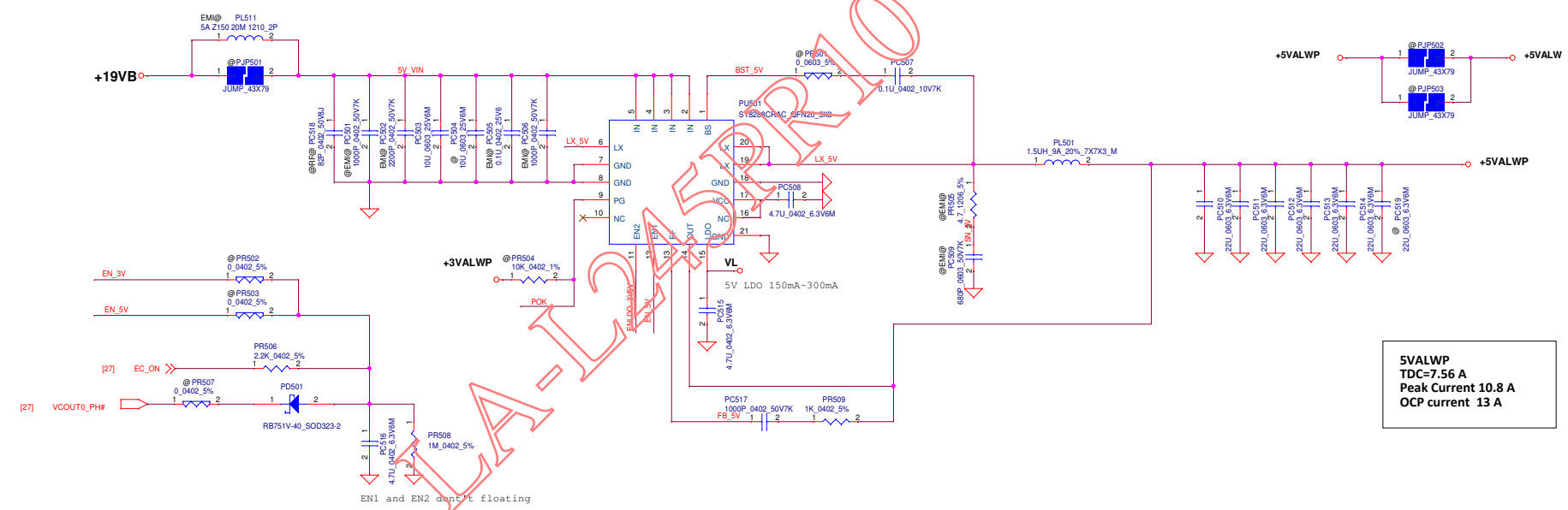
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Main Func = 3.3VALWP/5VALWP



3VALWP
TDC 5 A
Peak Current 7 A
OCP Current 8.4 A



5VALWP
TDC=7.56 A
Peak Current 10.8 A
OCP current 13 A

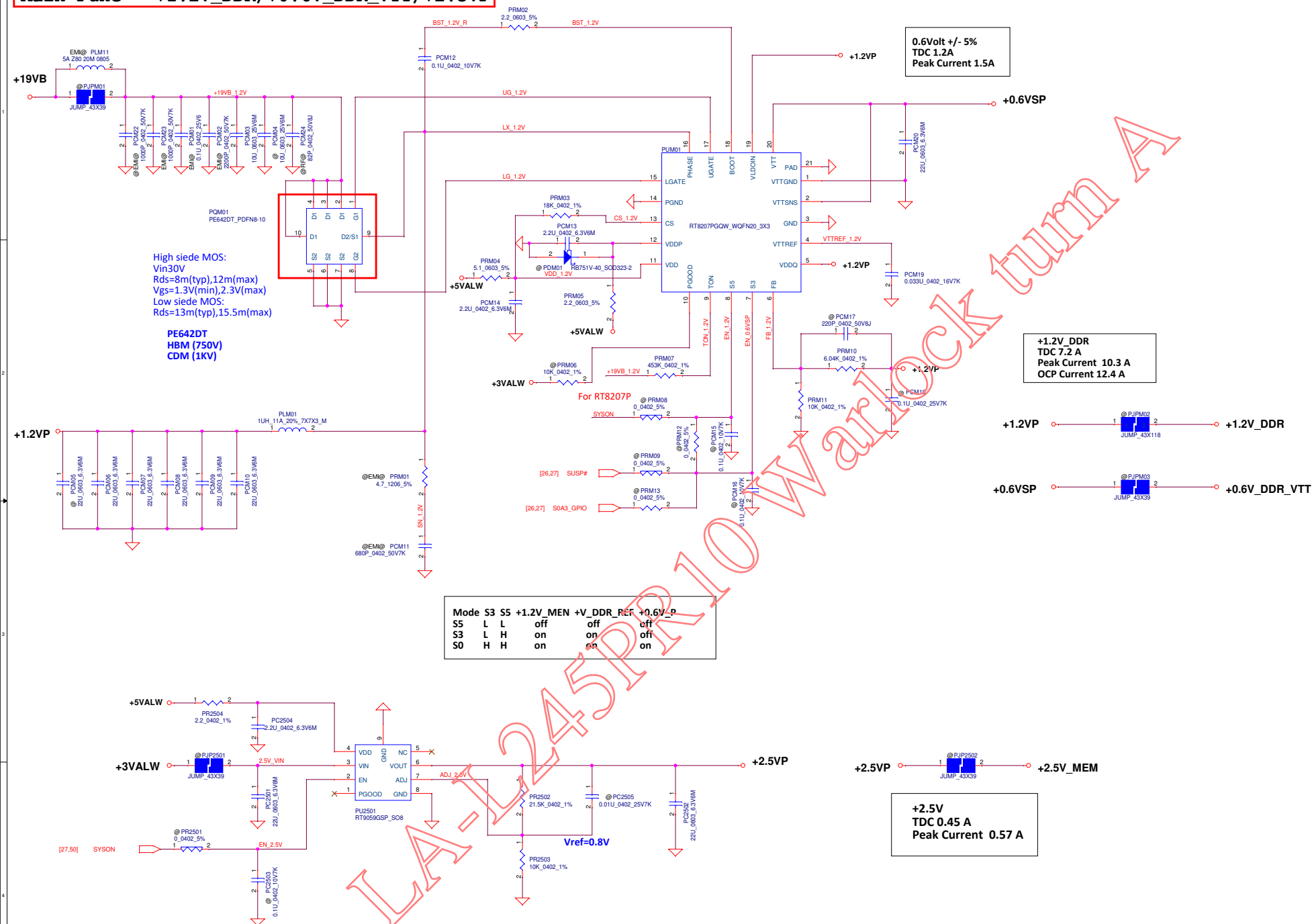
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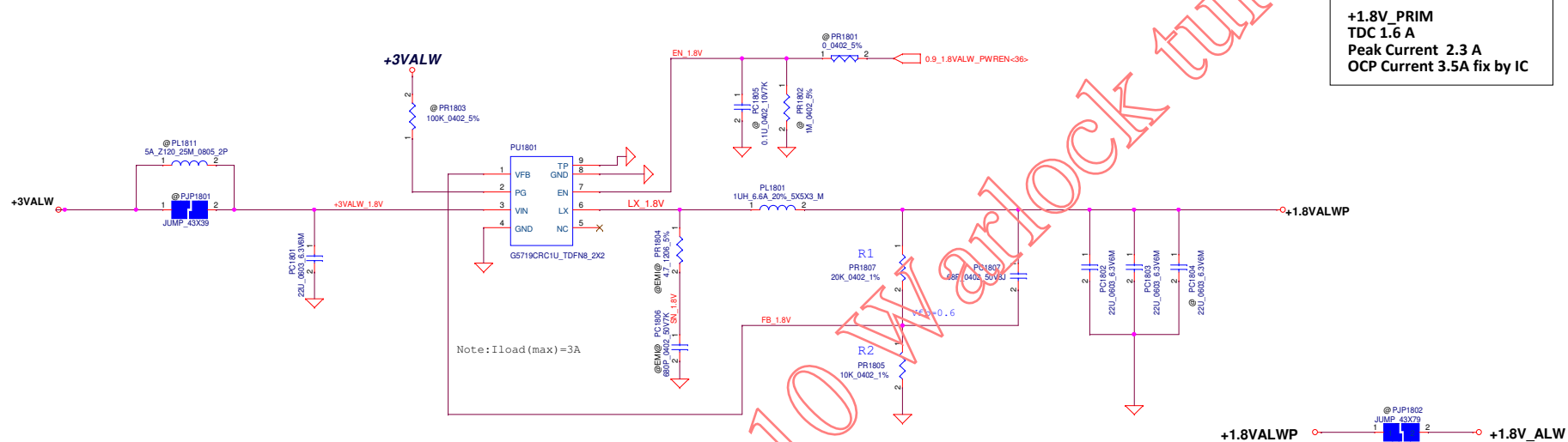
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Main Func = +1.2V_DDR/+0.6V_DDR_VTT/+2.5VP



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Main Func = +1.8VALWP



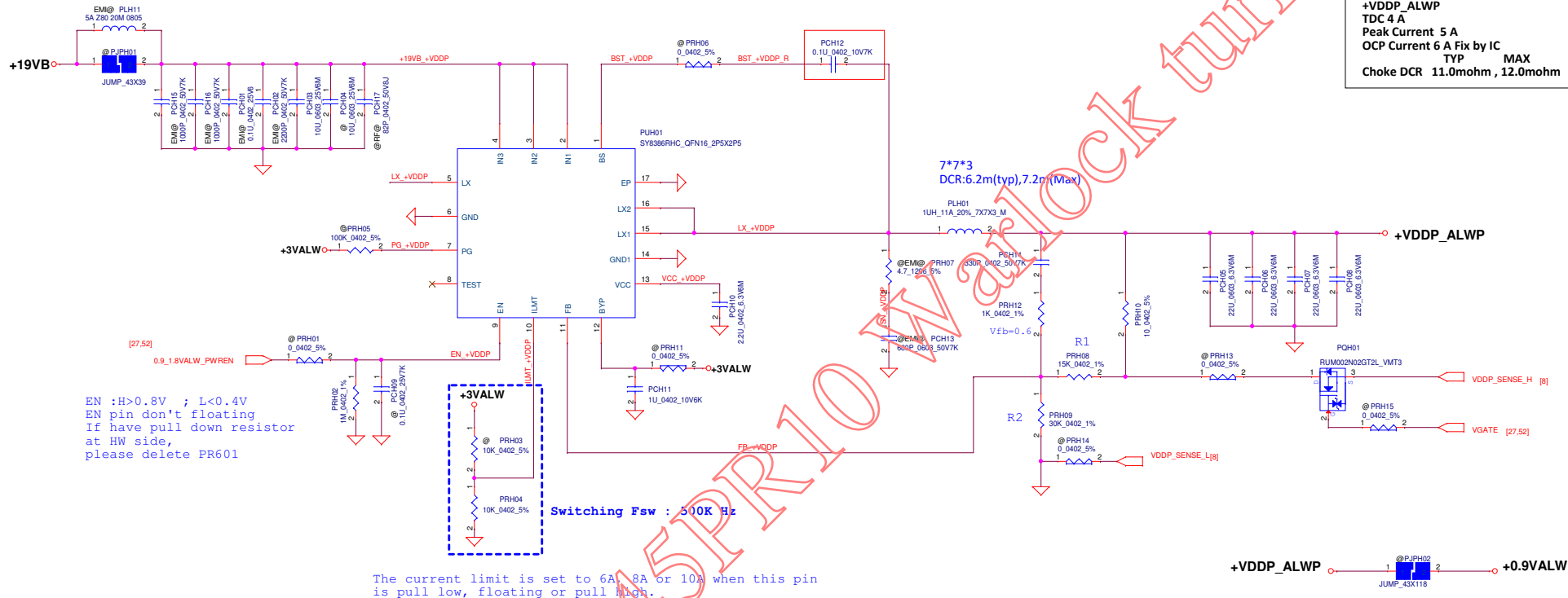
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Main Func = +VDDP_ALWP

The current limit is set to 6A, 8A or 10A when this pin is pull low, floating or pull high.

OCP setting	ILMT(pin3)
6A	Pull low
8A	Floating
10A	Pull high

+VDDP_ALWP
TDC 4 A
Peak Current 5 A
OCP Current 6 A Fix by IC
TYP MAX
Choke DCR 11.0mohm , 12.0mohm



EN :H>0.8V ; L<0.4V
EN pin don't floating
If have pull down resistor
at HW side,
please delete PR601

The current limit is set to 6A, 8A or 10A when this pin is pull low, floating or pull high.

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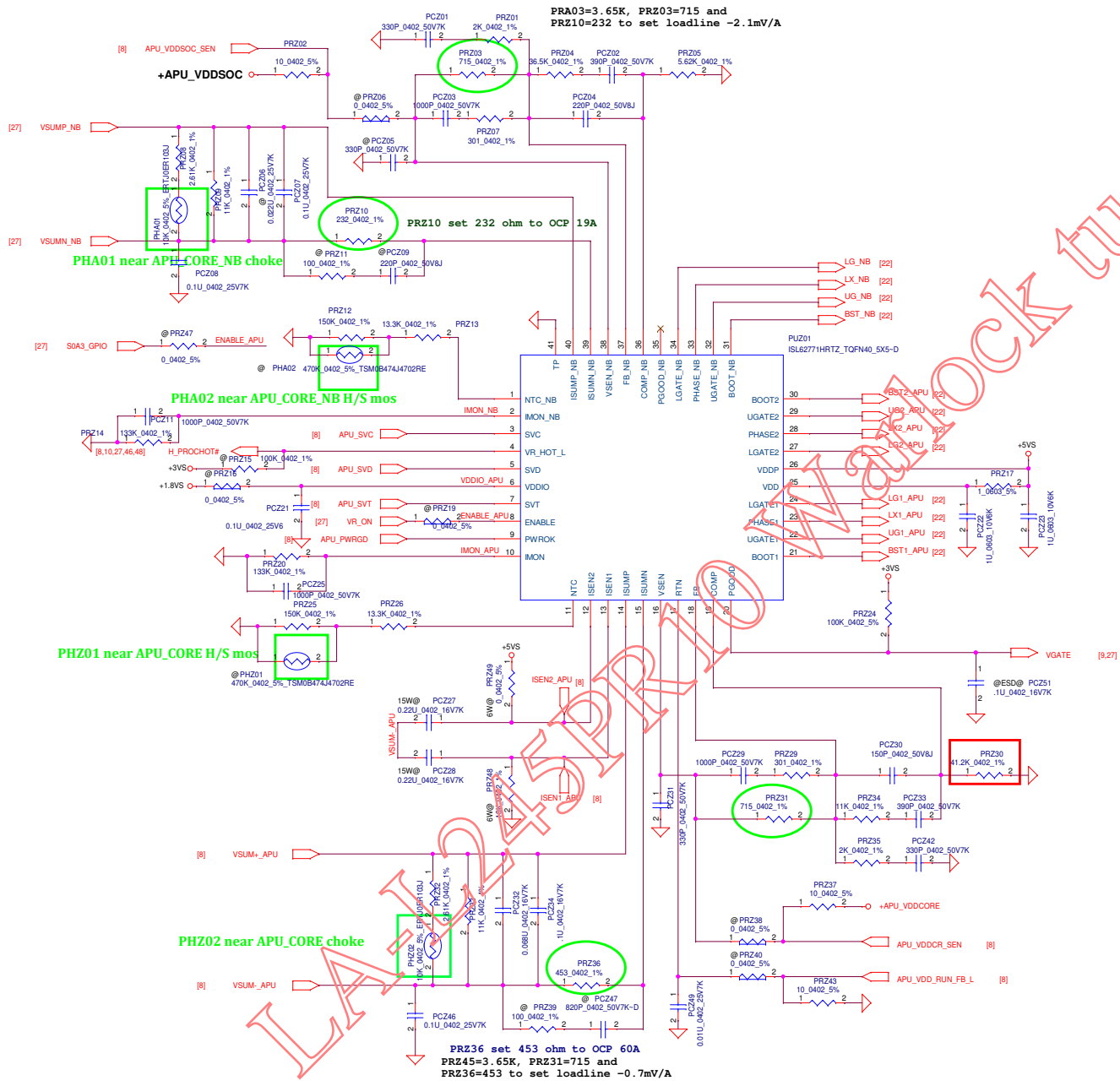
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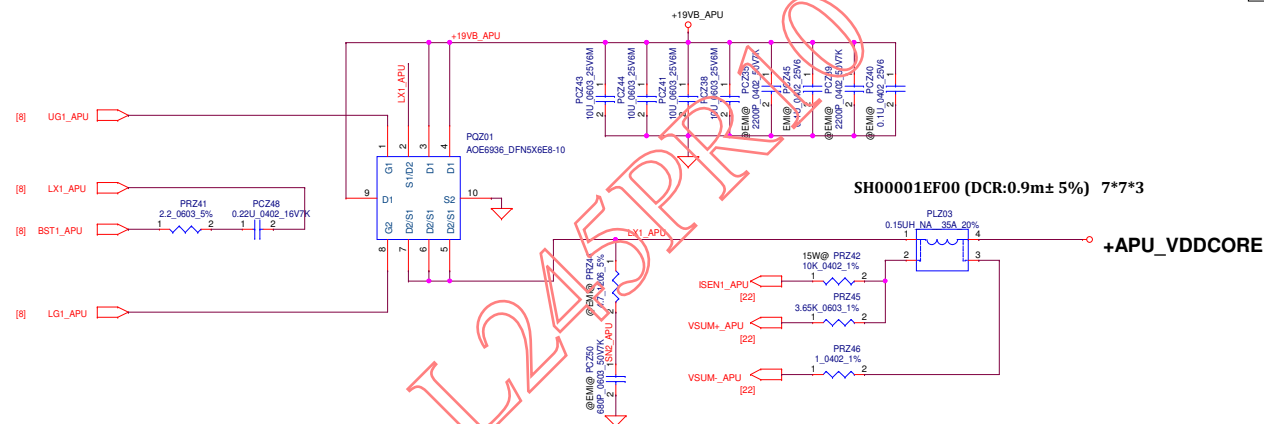
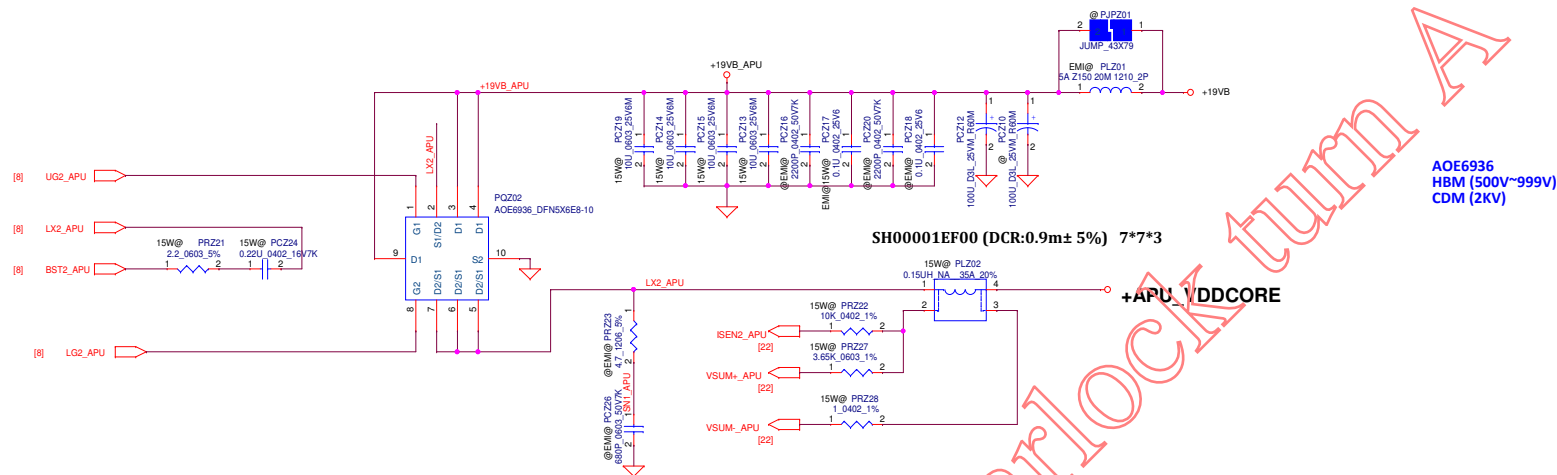
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				PWR APU CORE IC			
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Main Func = APU_CORE_SW



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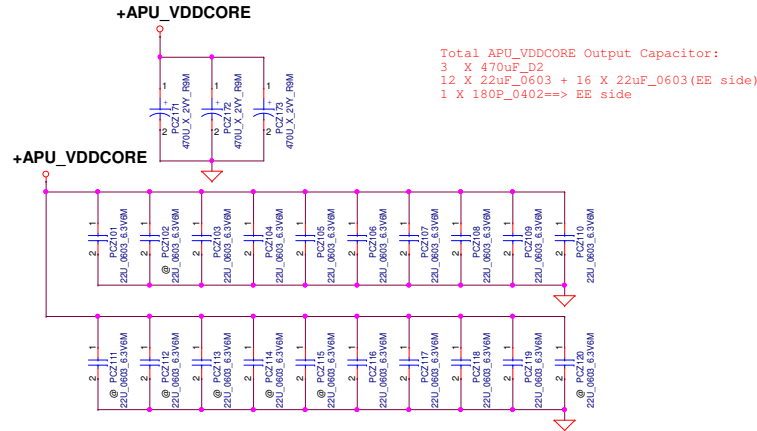
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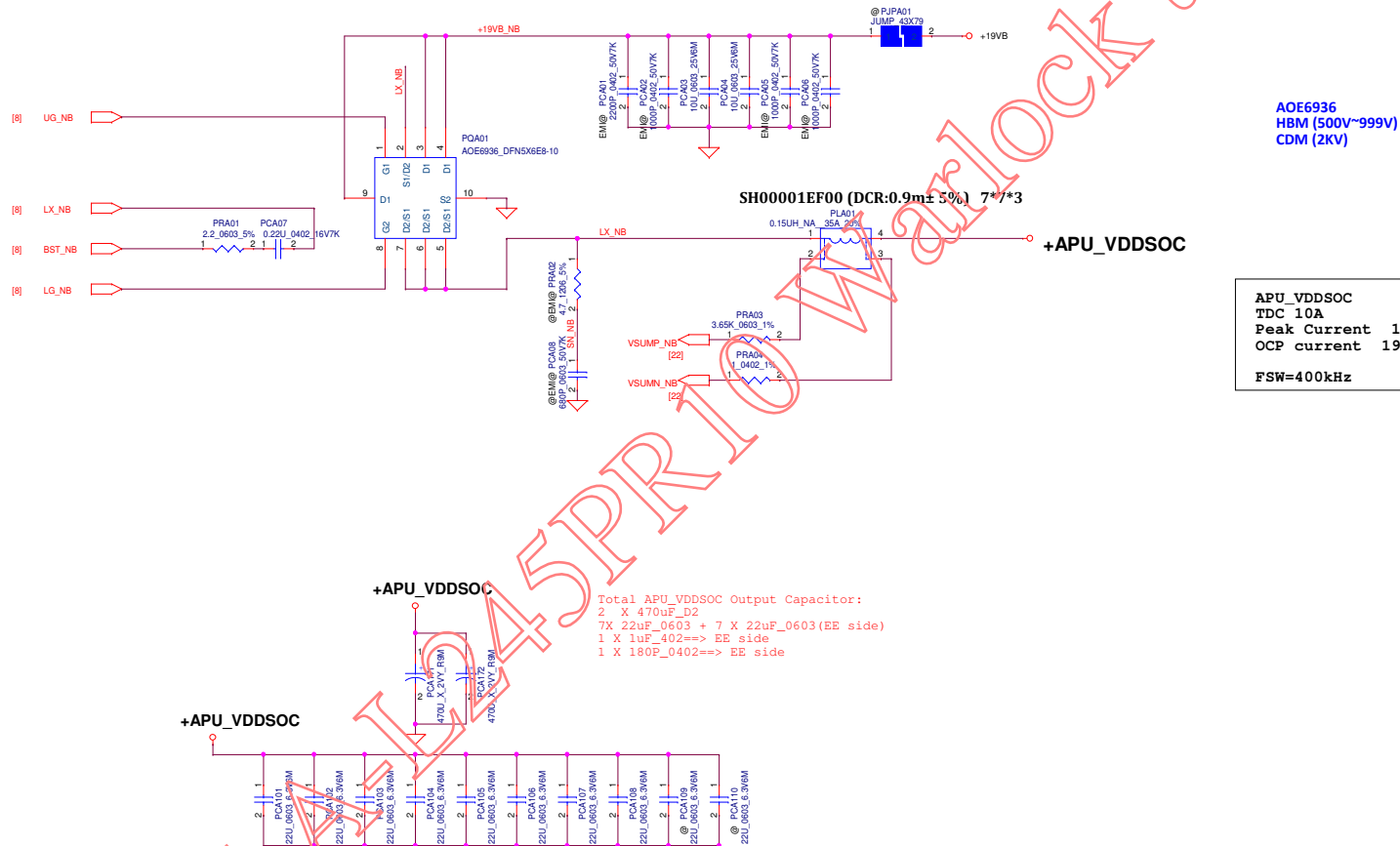
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